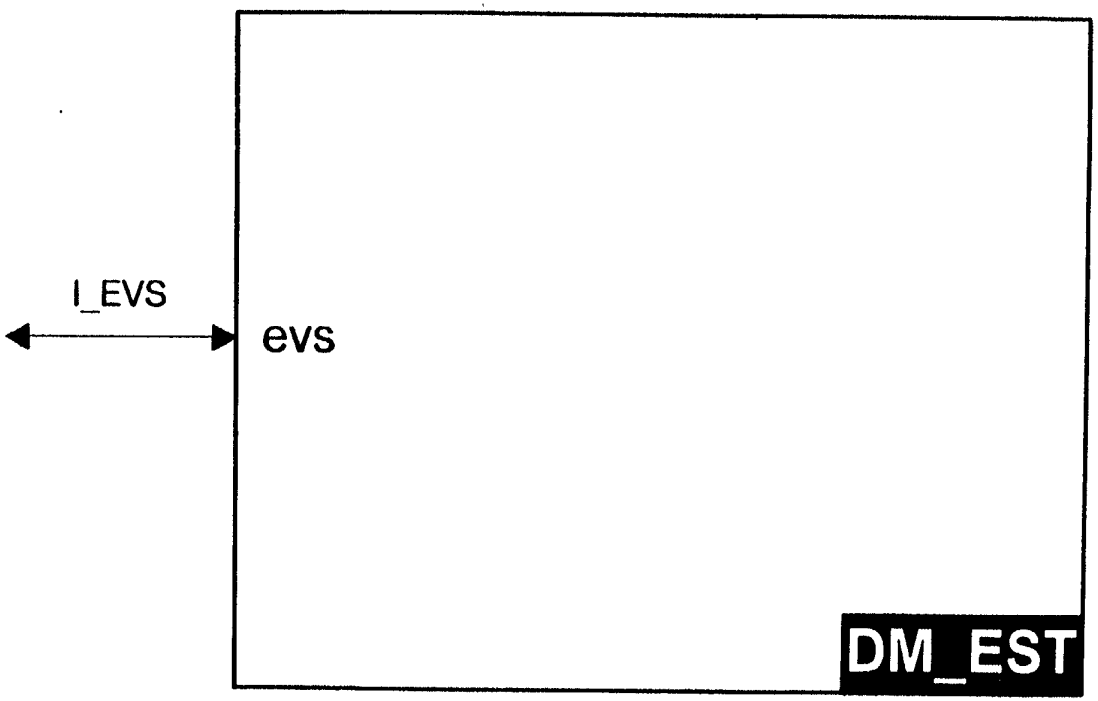


Fig. 1

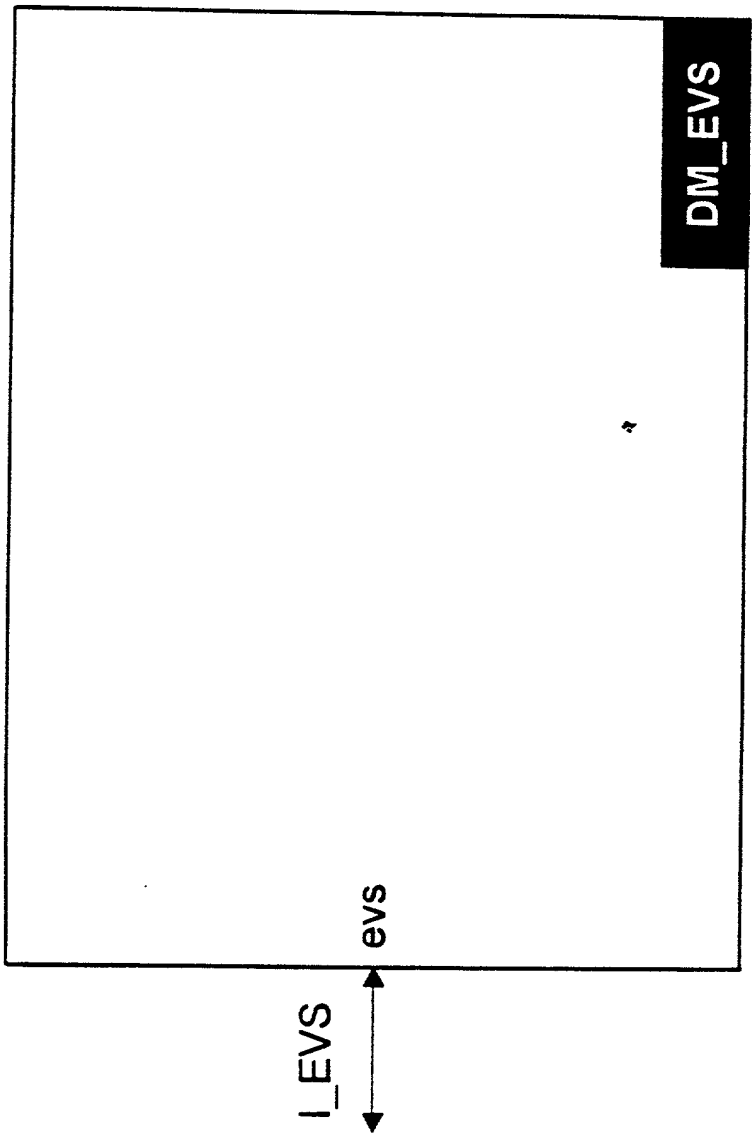


Fig. 2

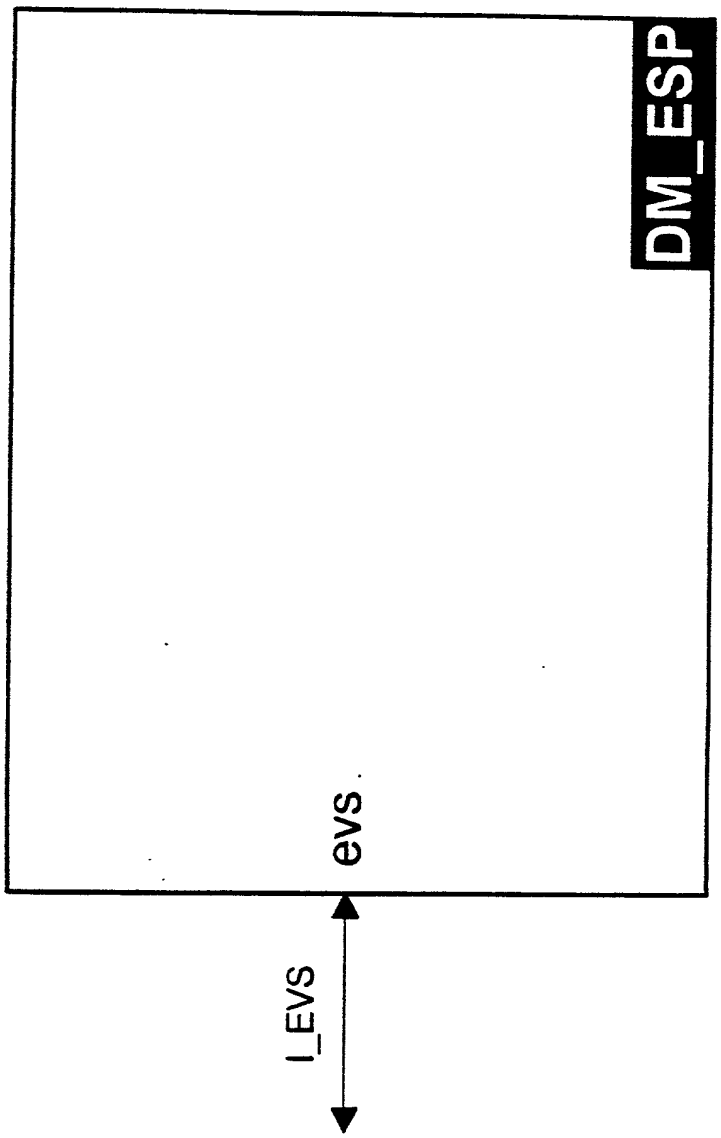


Fig. 3

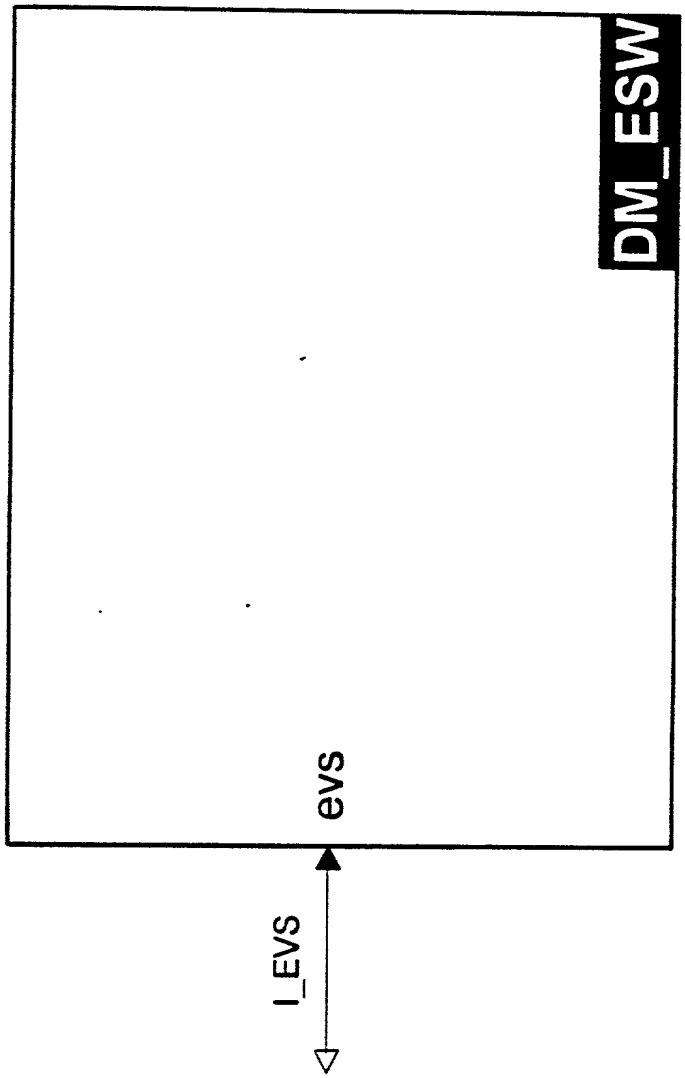


Fig. 4

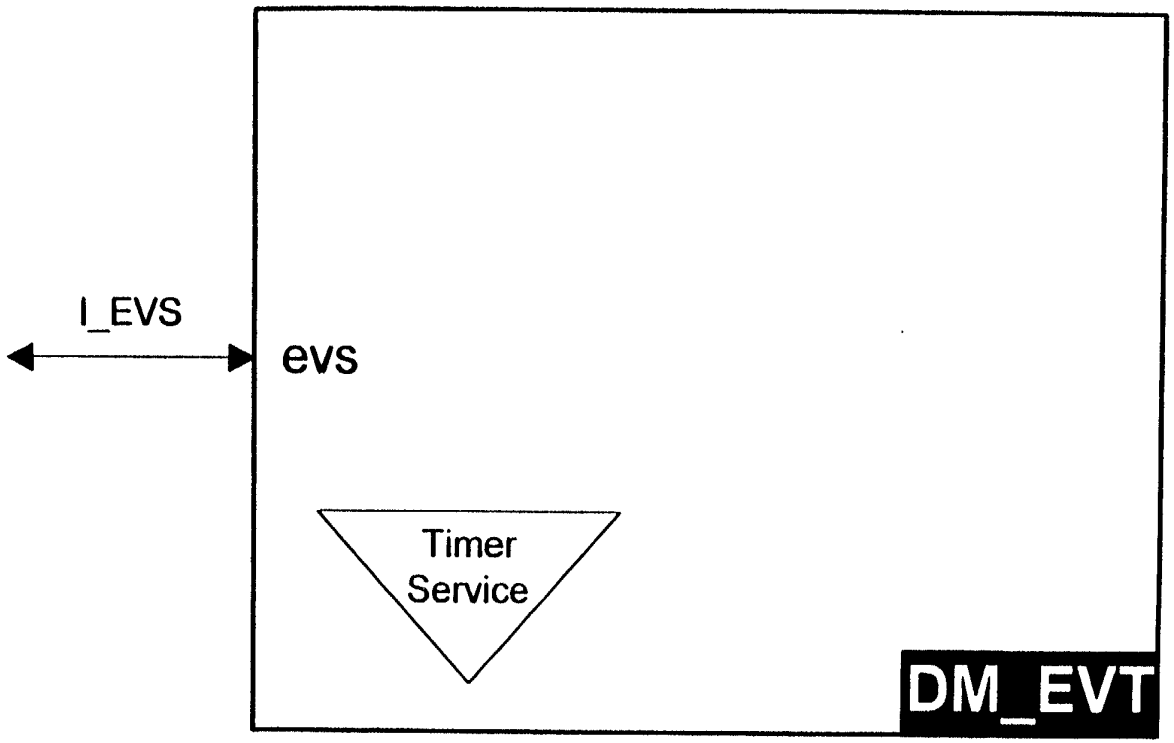


Fig. 5

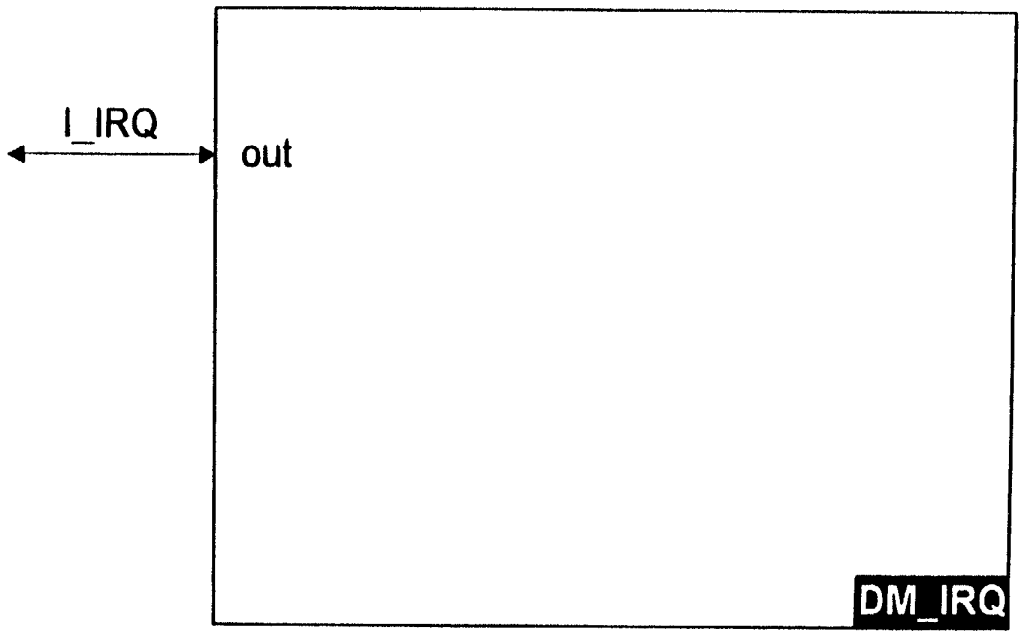


Fig. 6

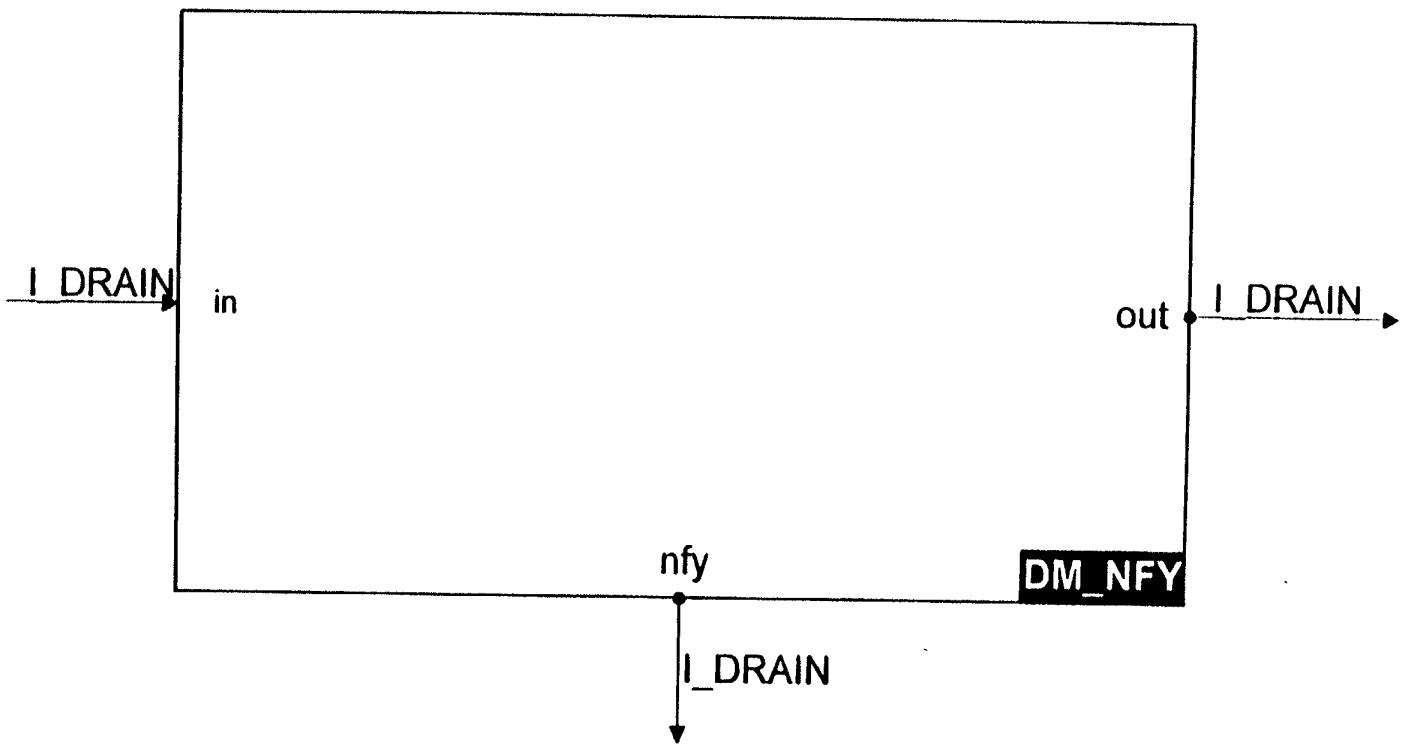


Fig. 7

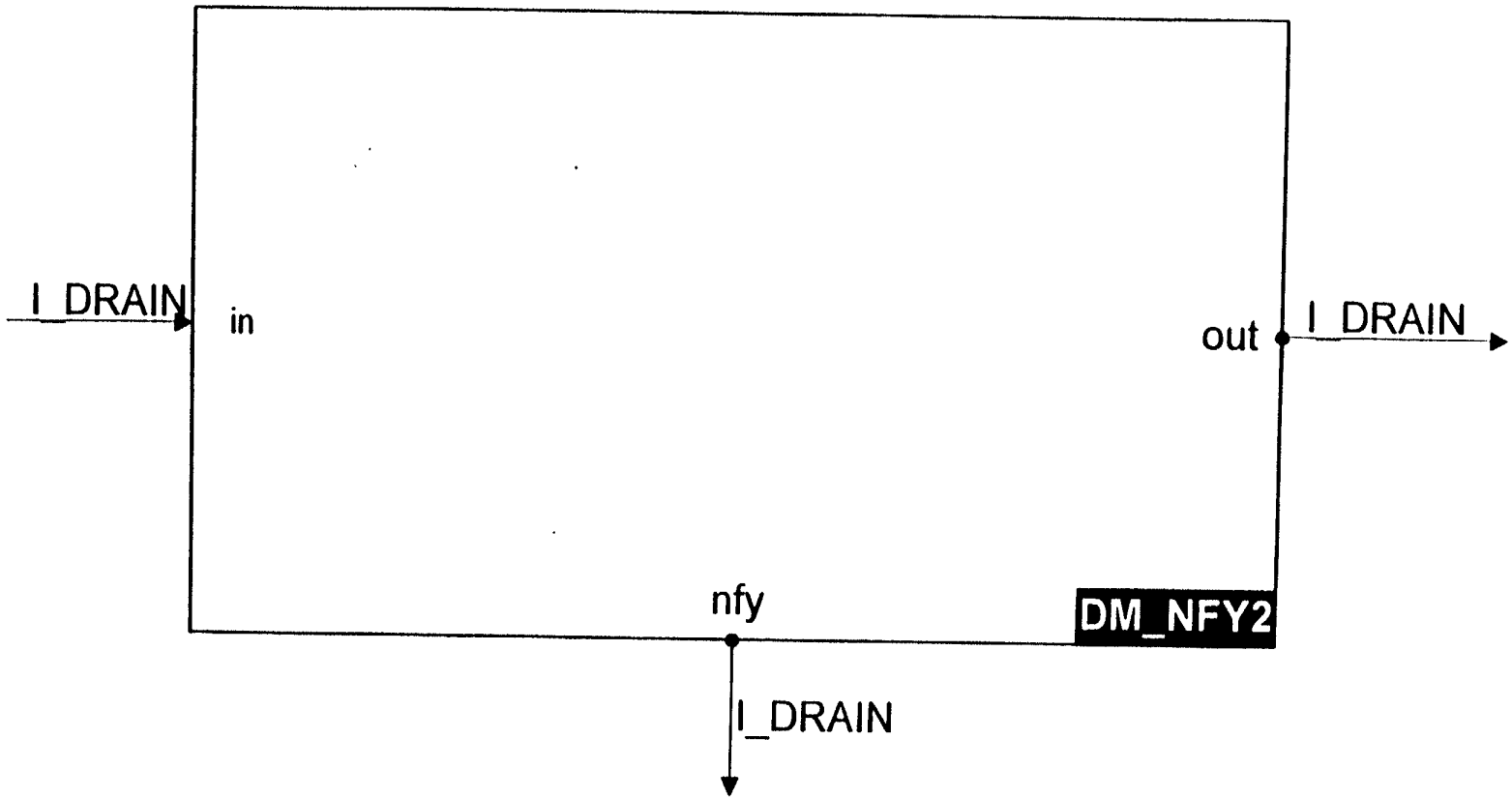
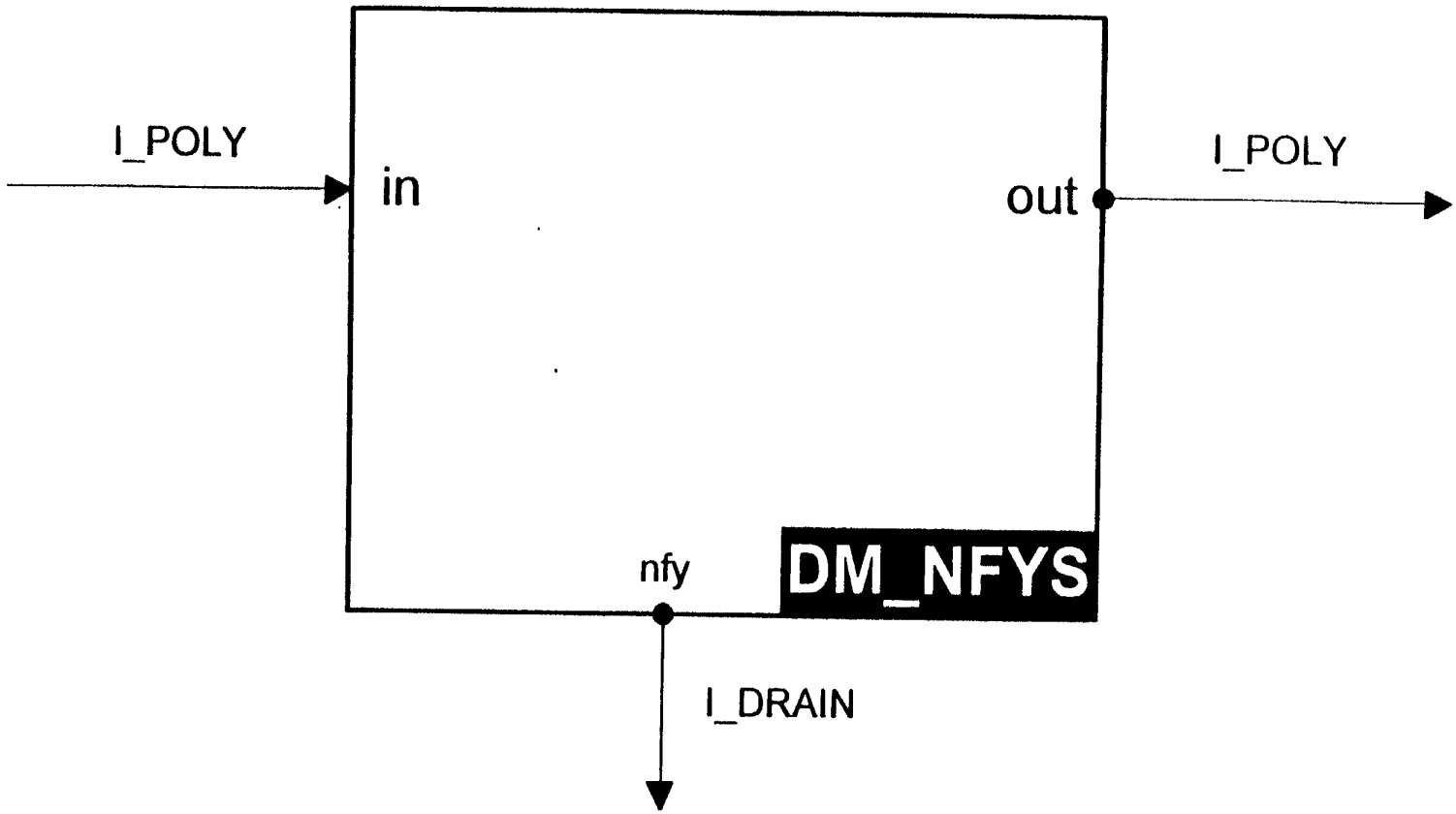


Fig. 8



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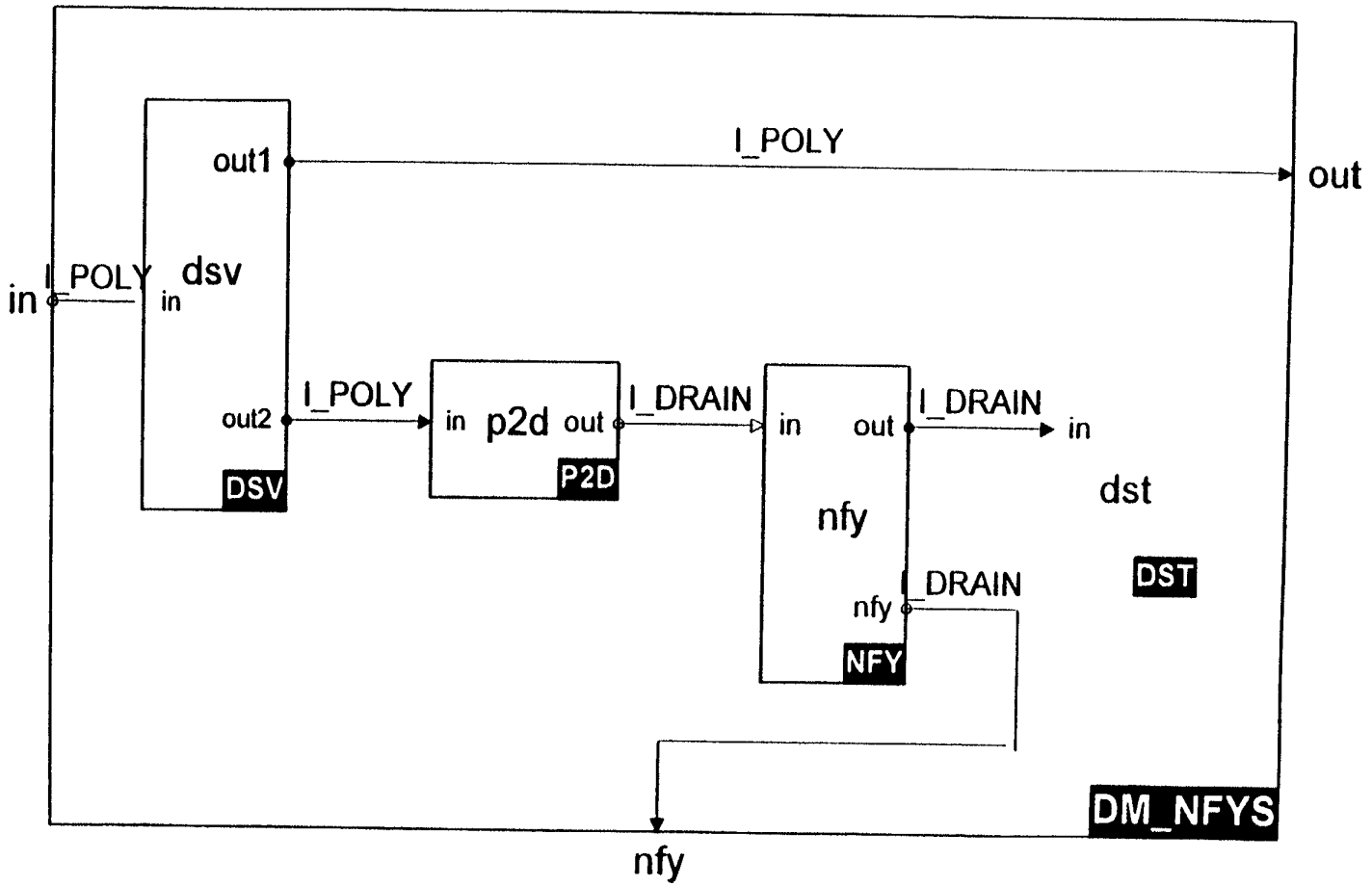
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nfy
NFY
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nfy

Fig. 10

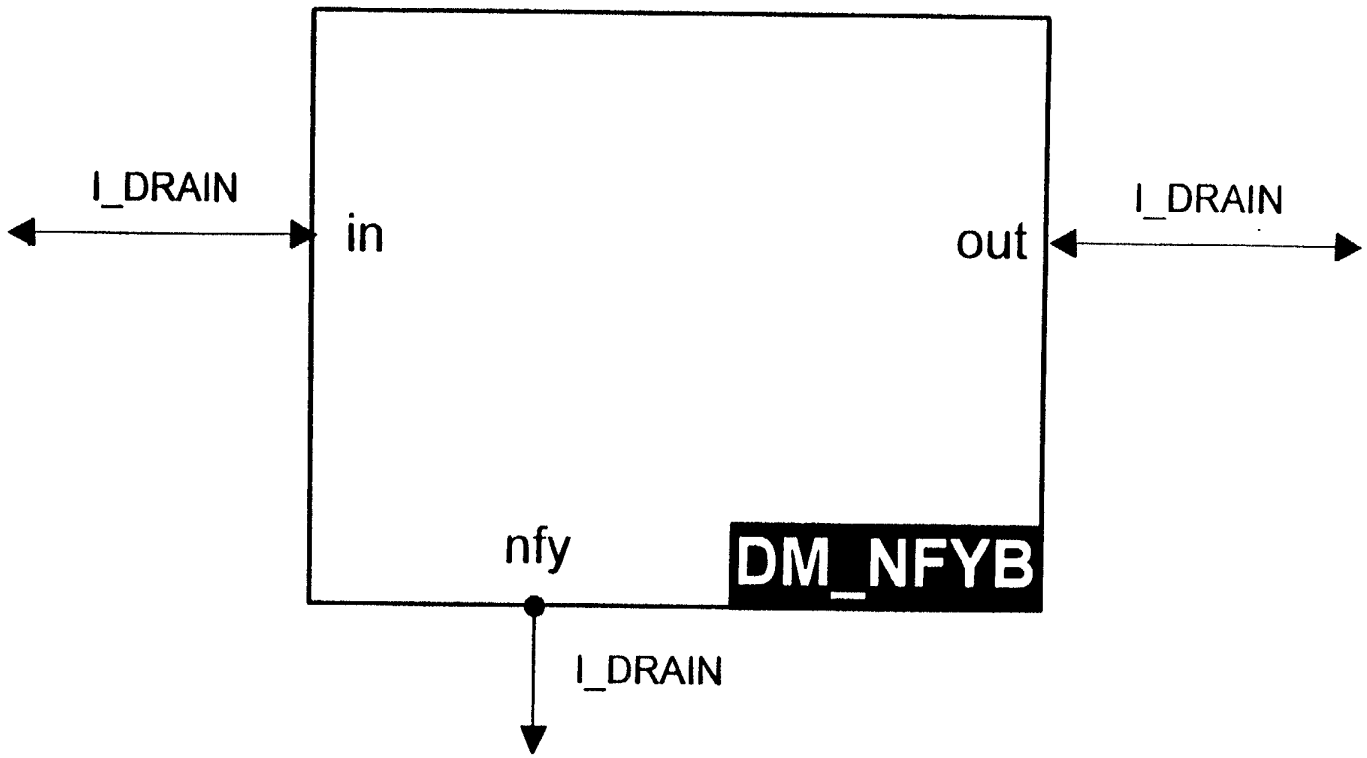
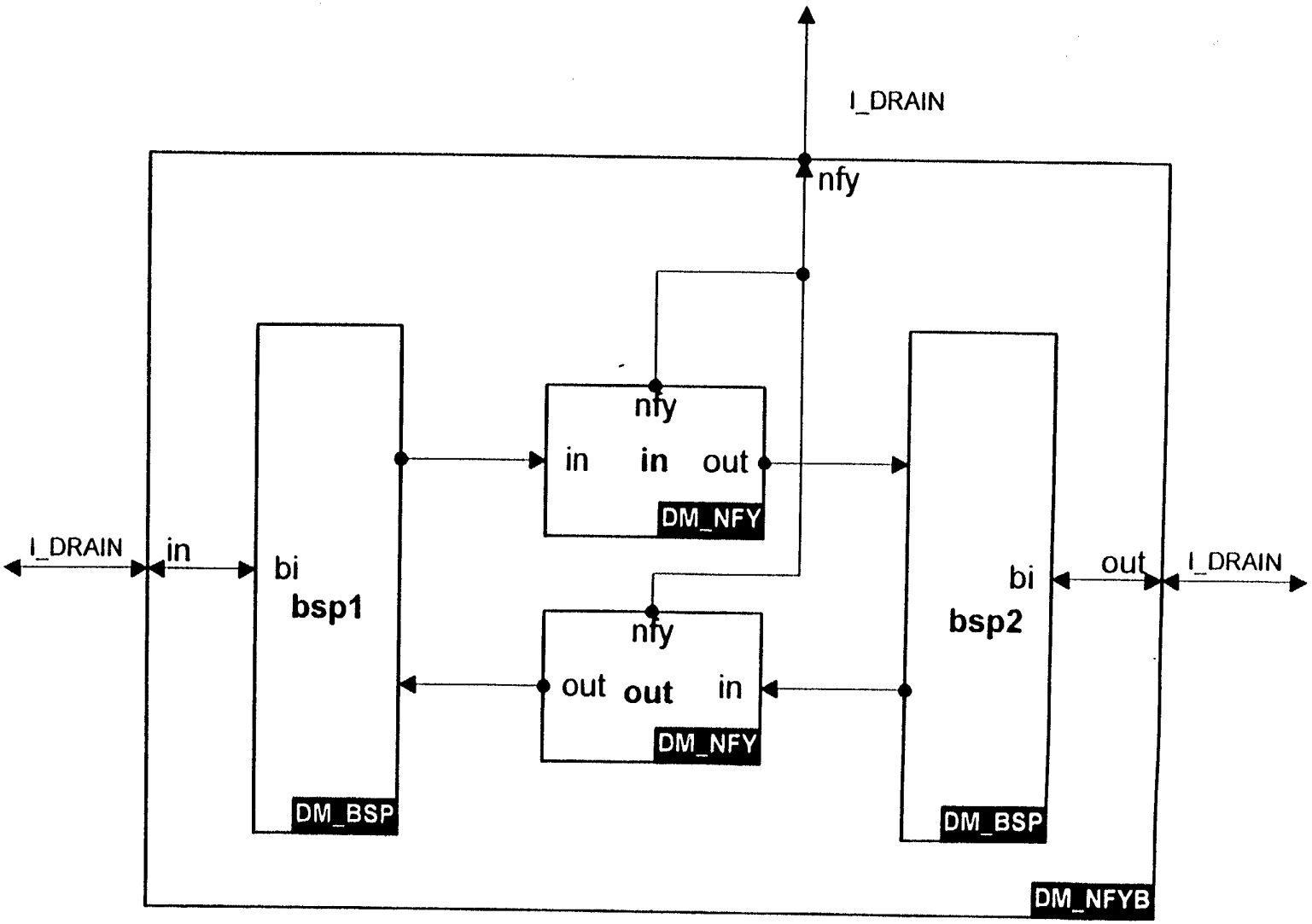


Fig. 11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DM_NFYB

Fig. 12

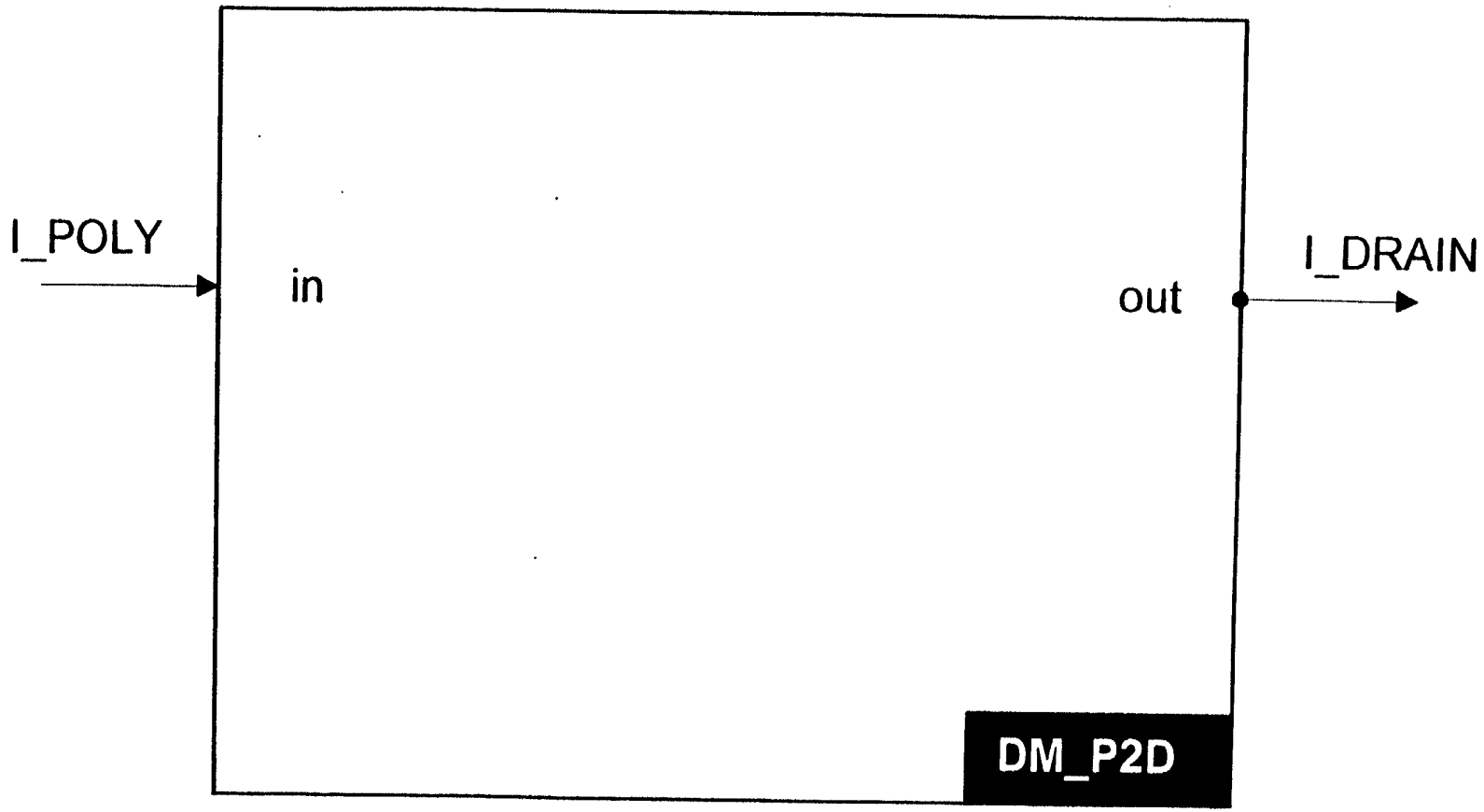


Fig. 13

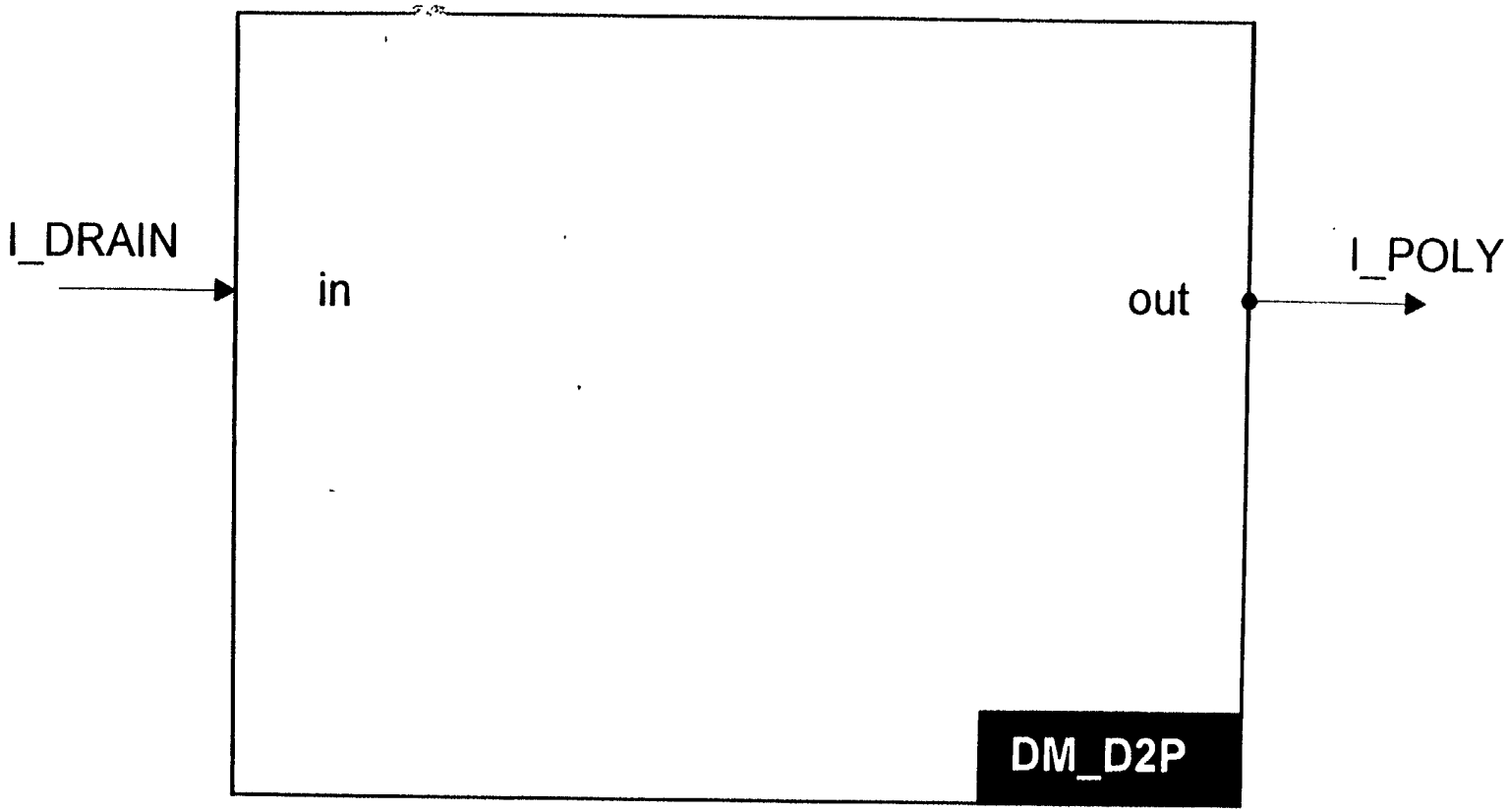


Fig. 14

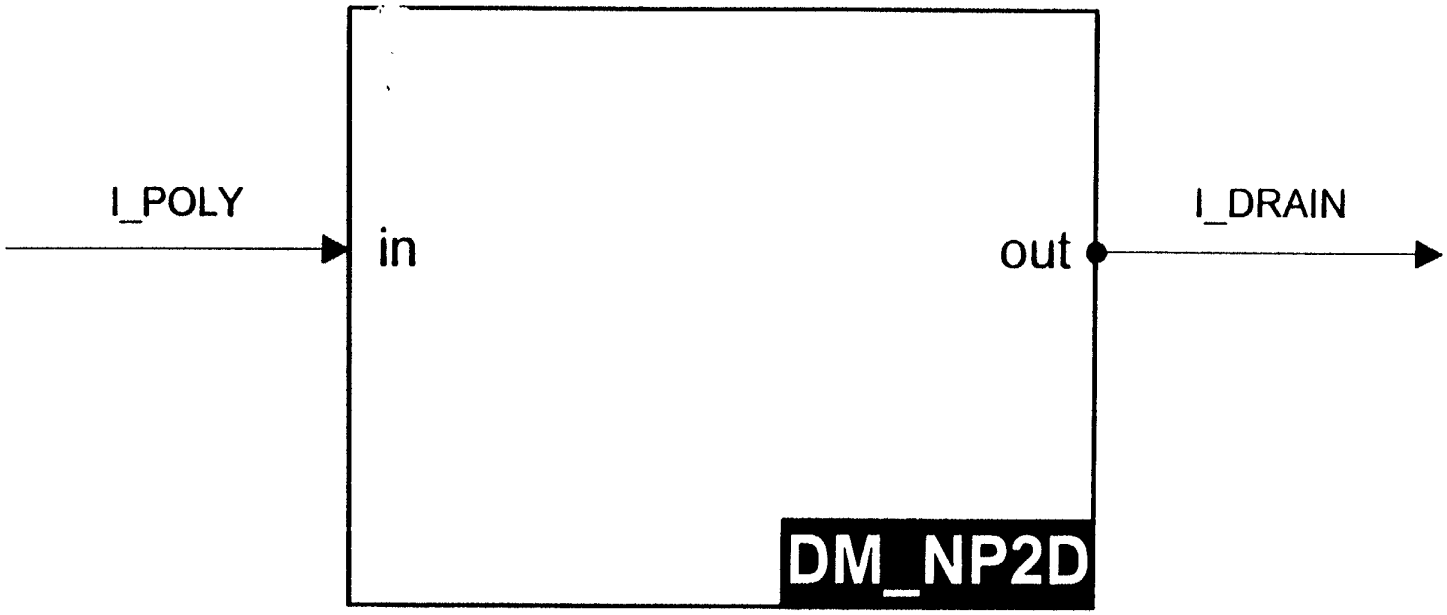


Fig. 15

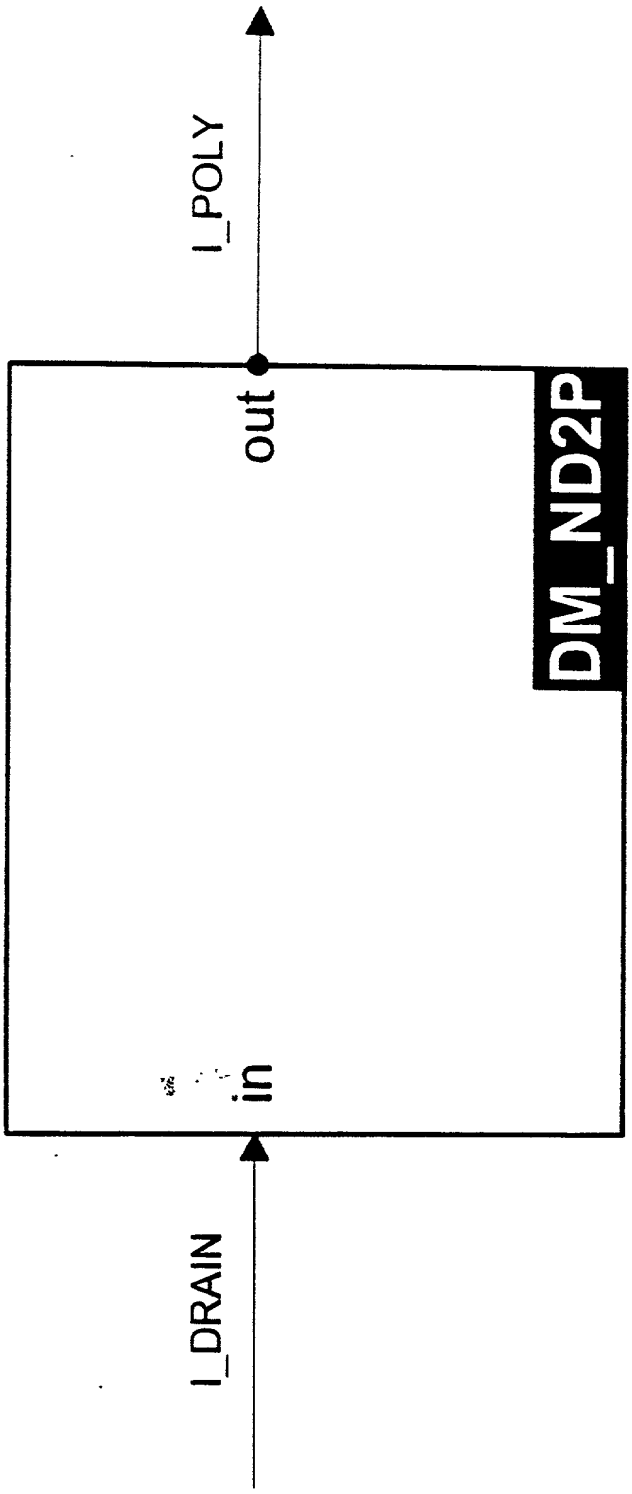


Fig. 16

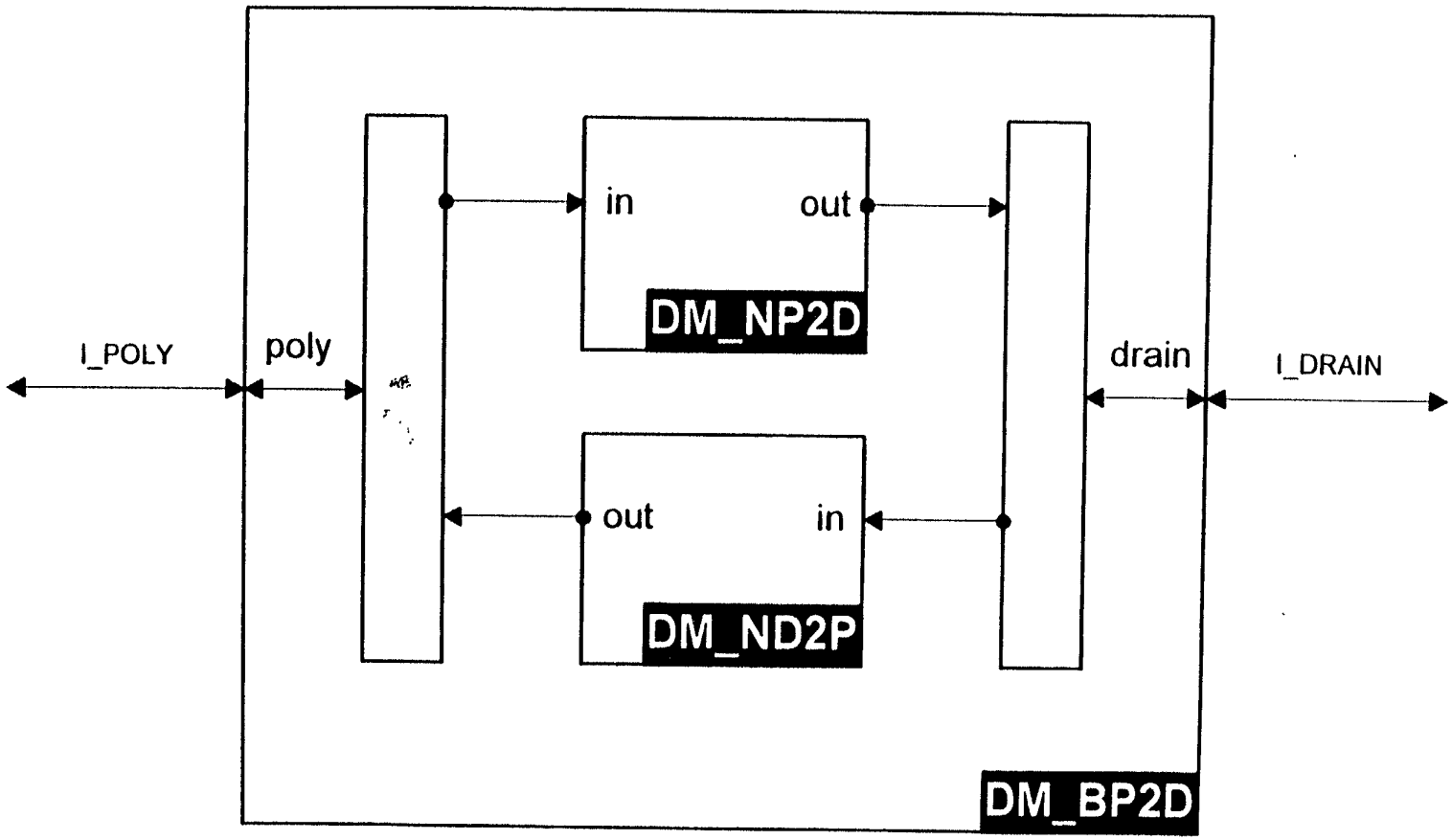


Fig. 17

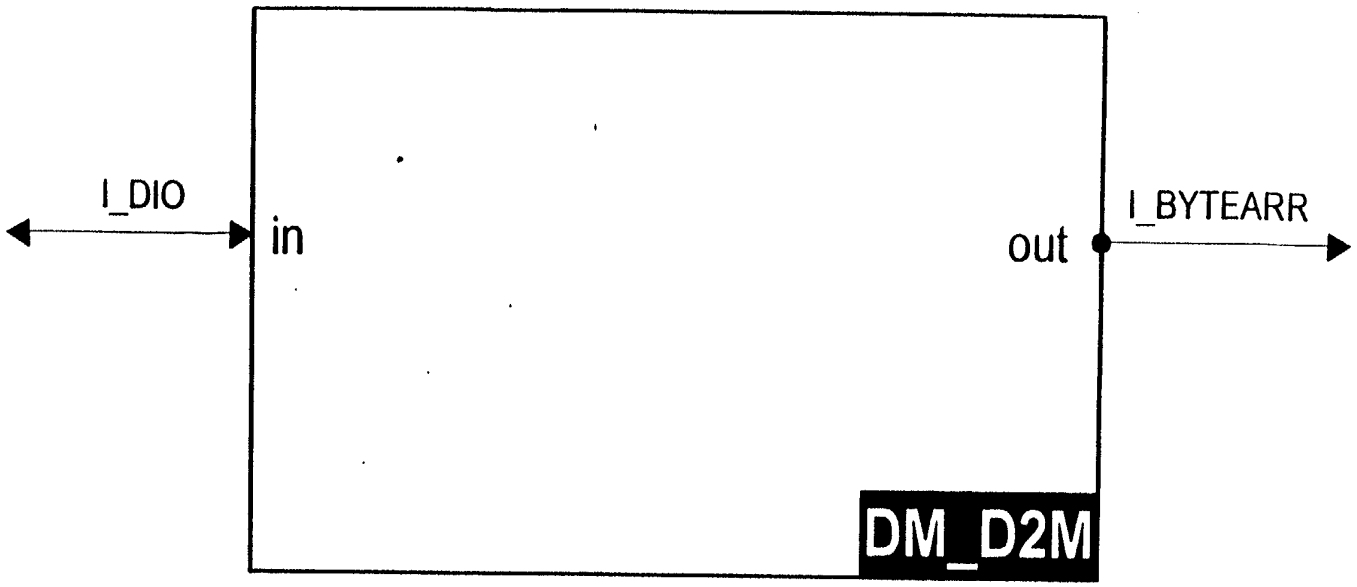
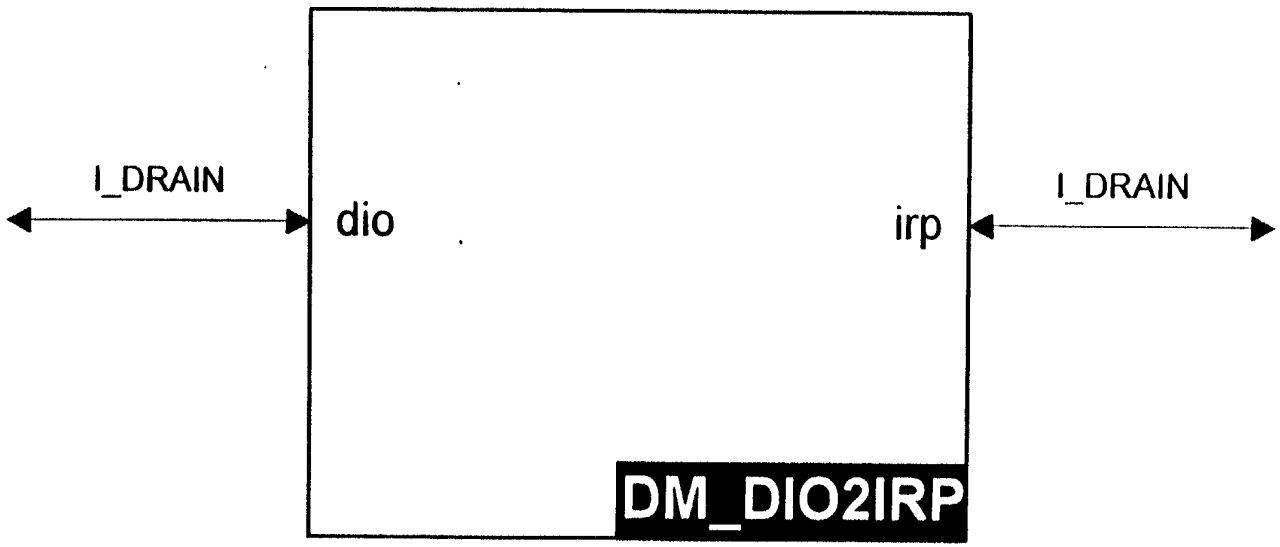


Fig. 18



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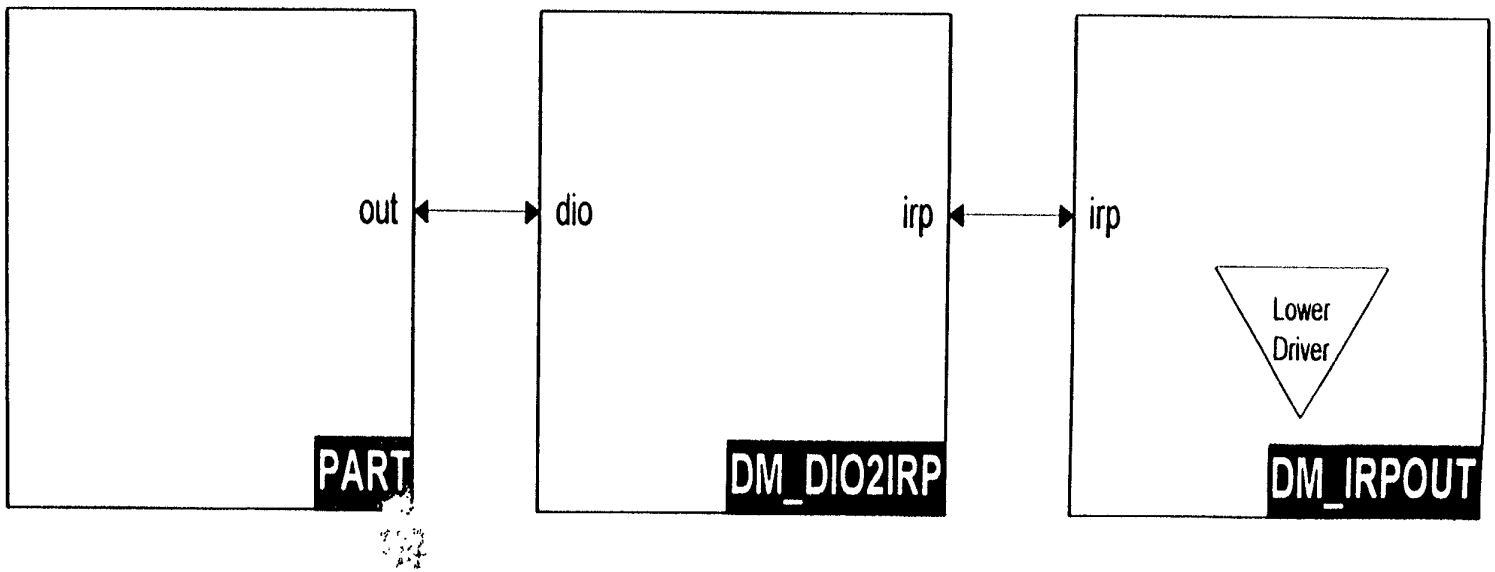


Fig. 20

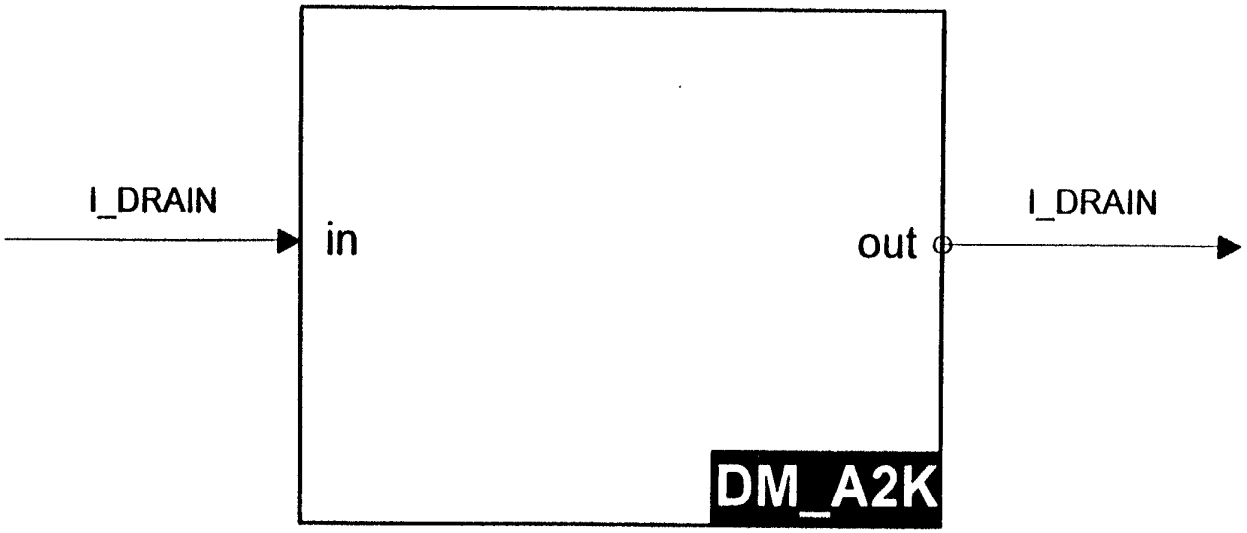


Fig. 21

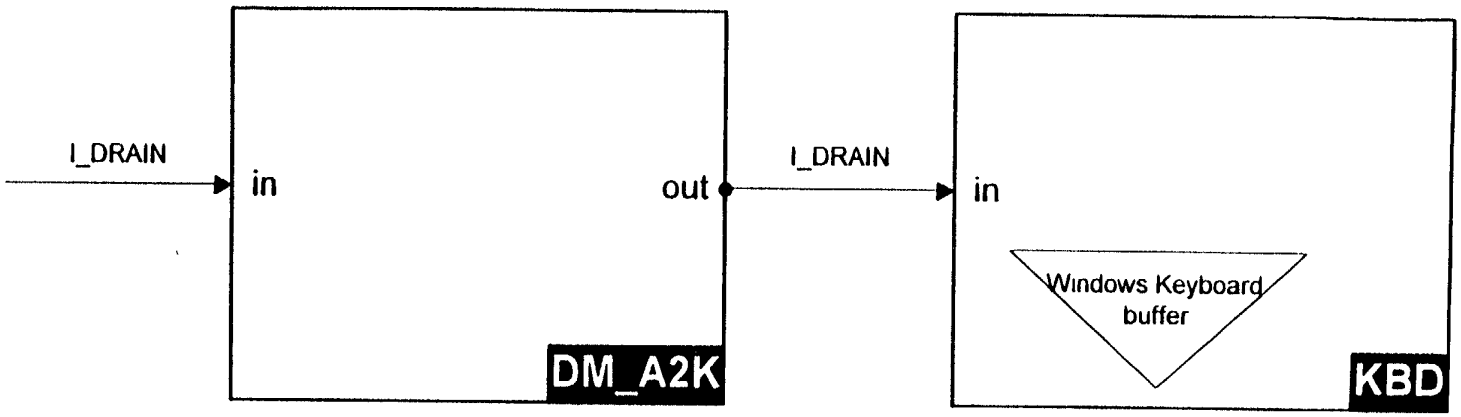


Fig. 22

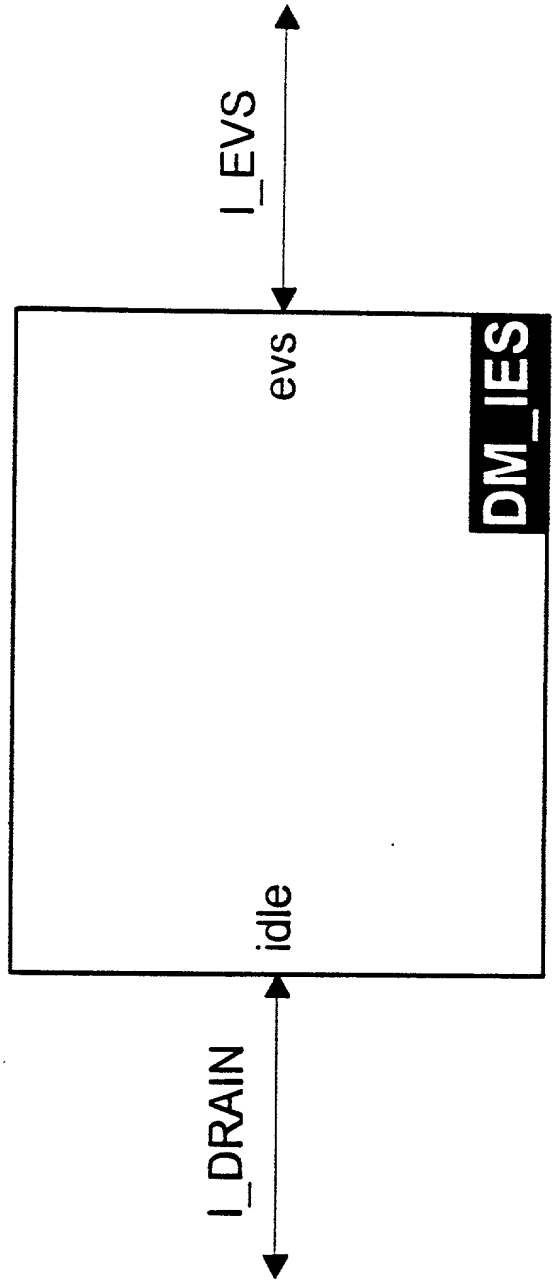


Fig. 23

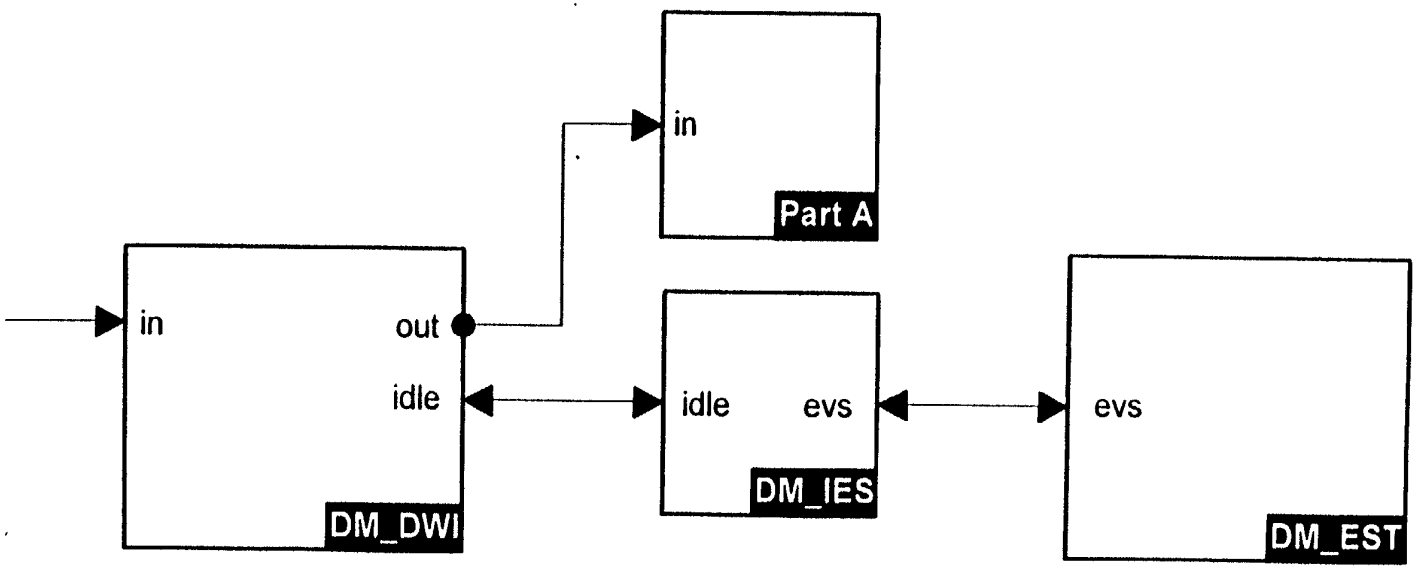


Fig. 24

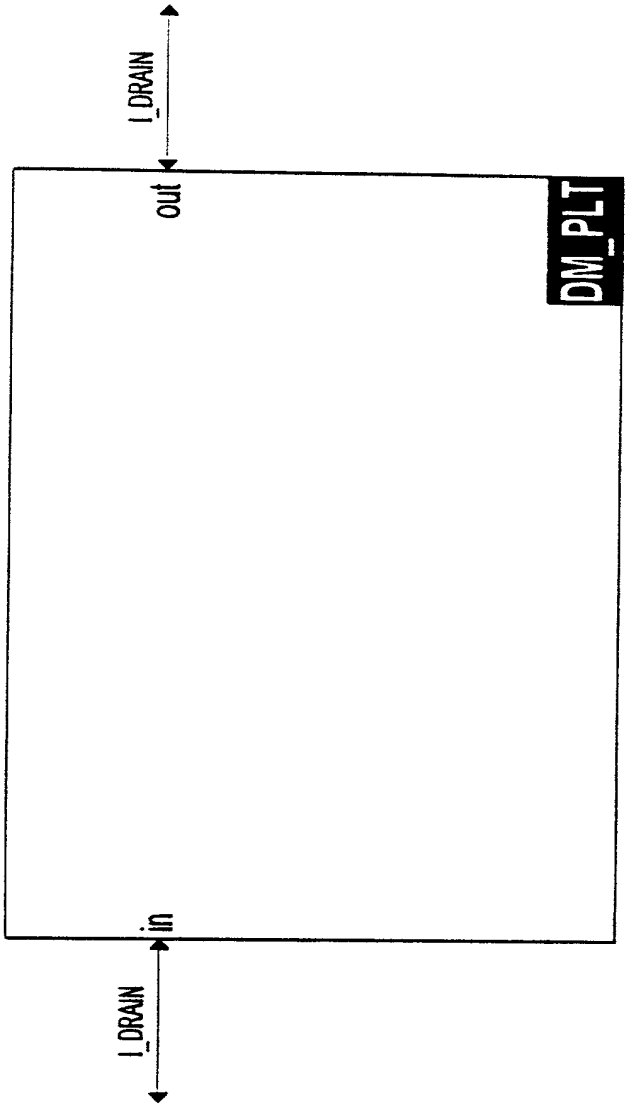


Fig. 25

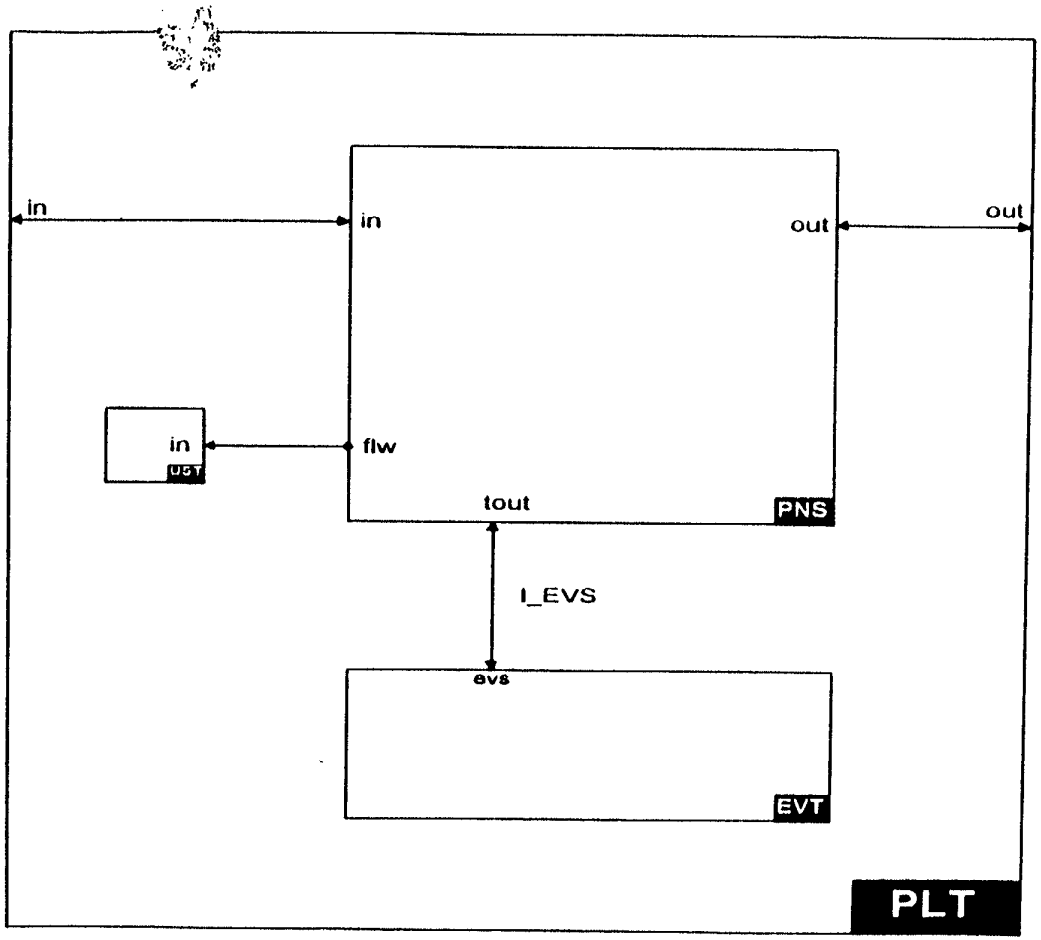


Fig. 26

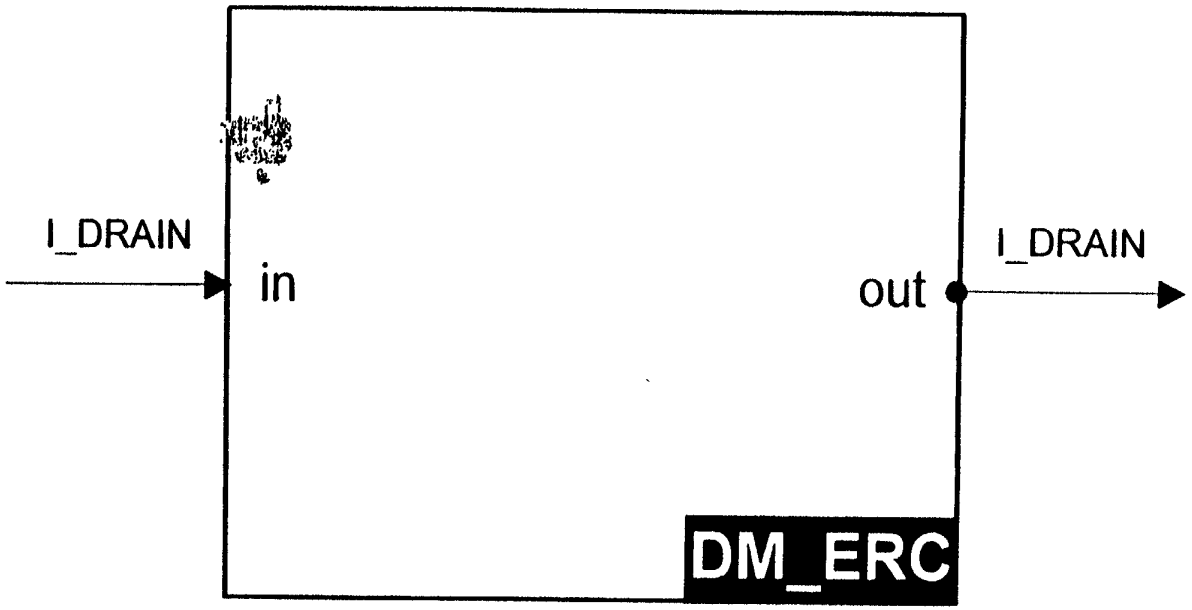


Fig. 27

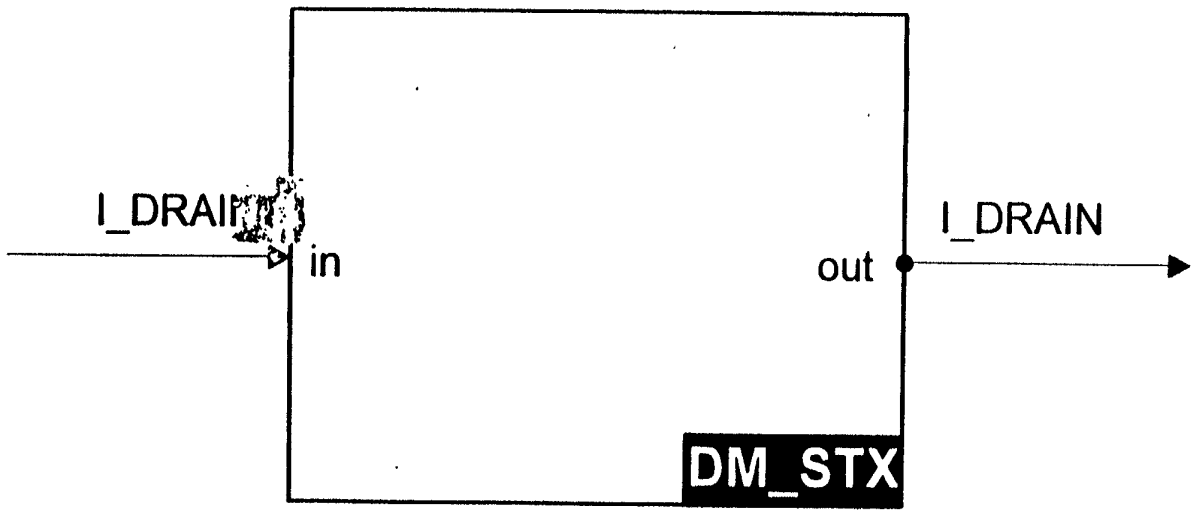


Fig. 28

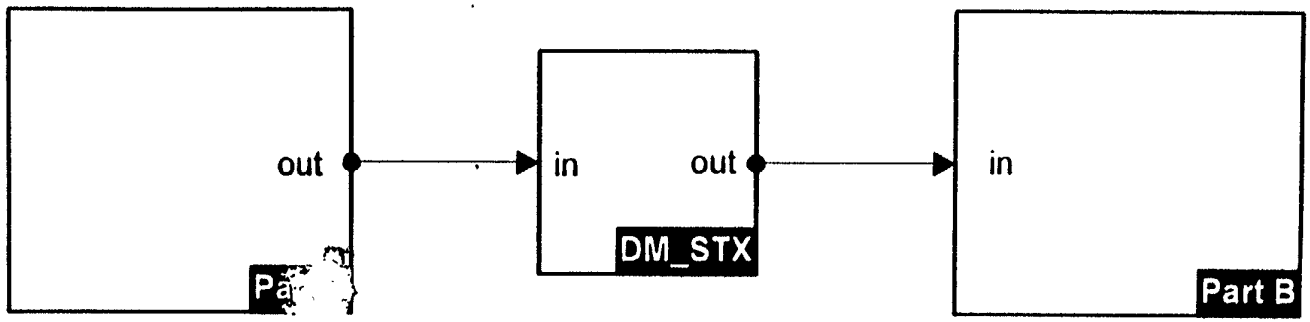


Fig. 29

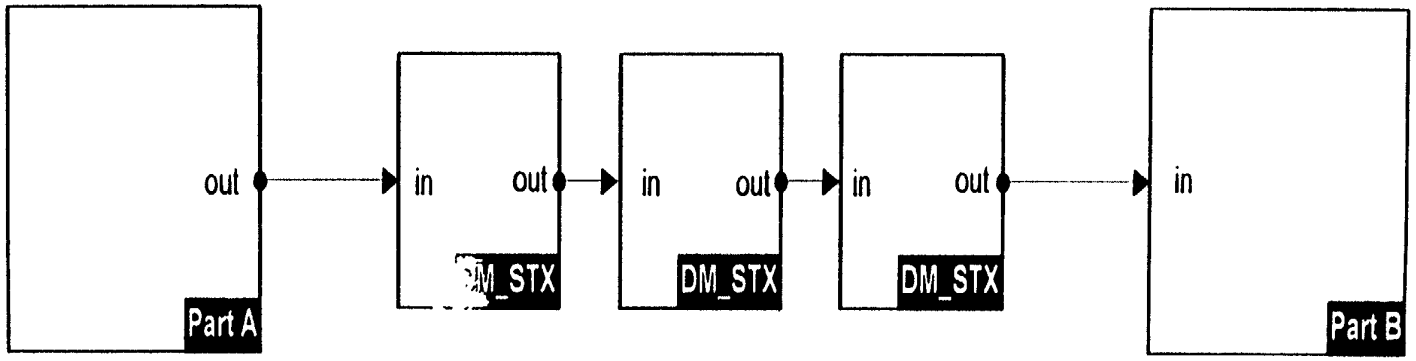


Fig. 30

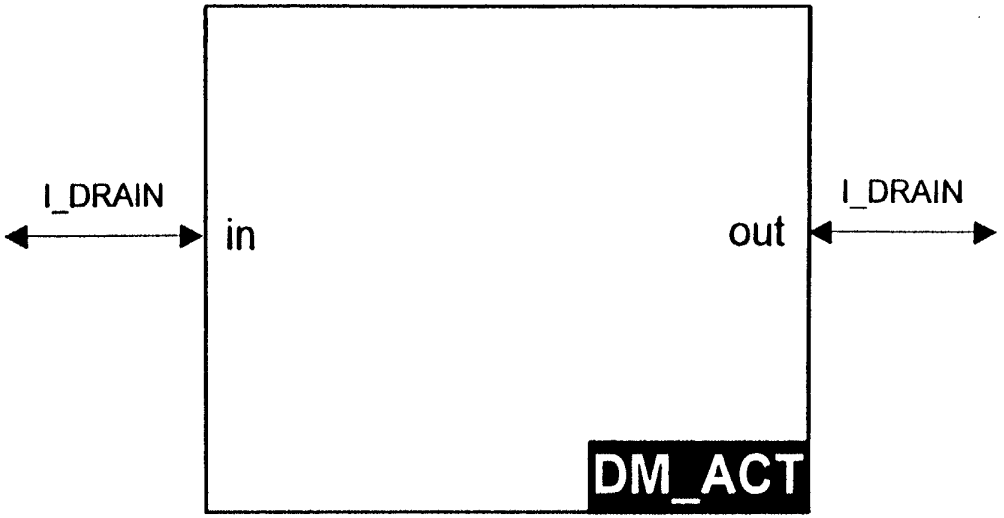


Fig. 31

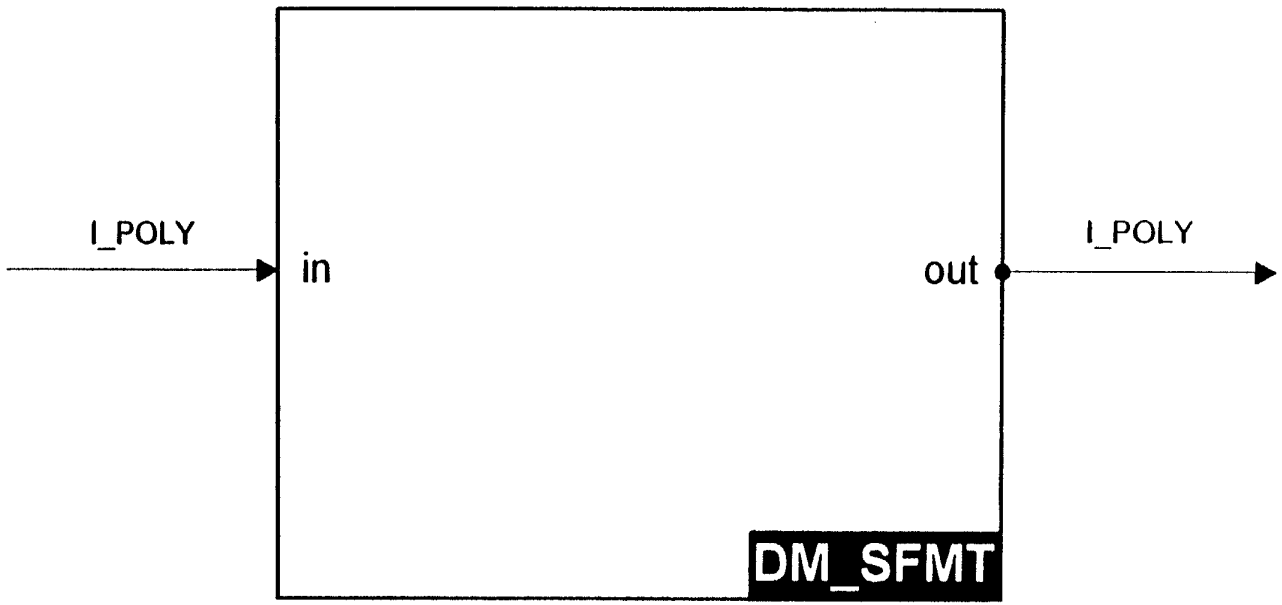


Fig. 32

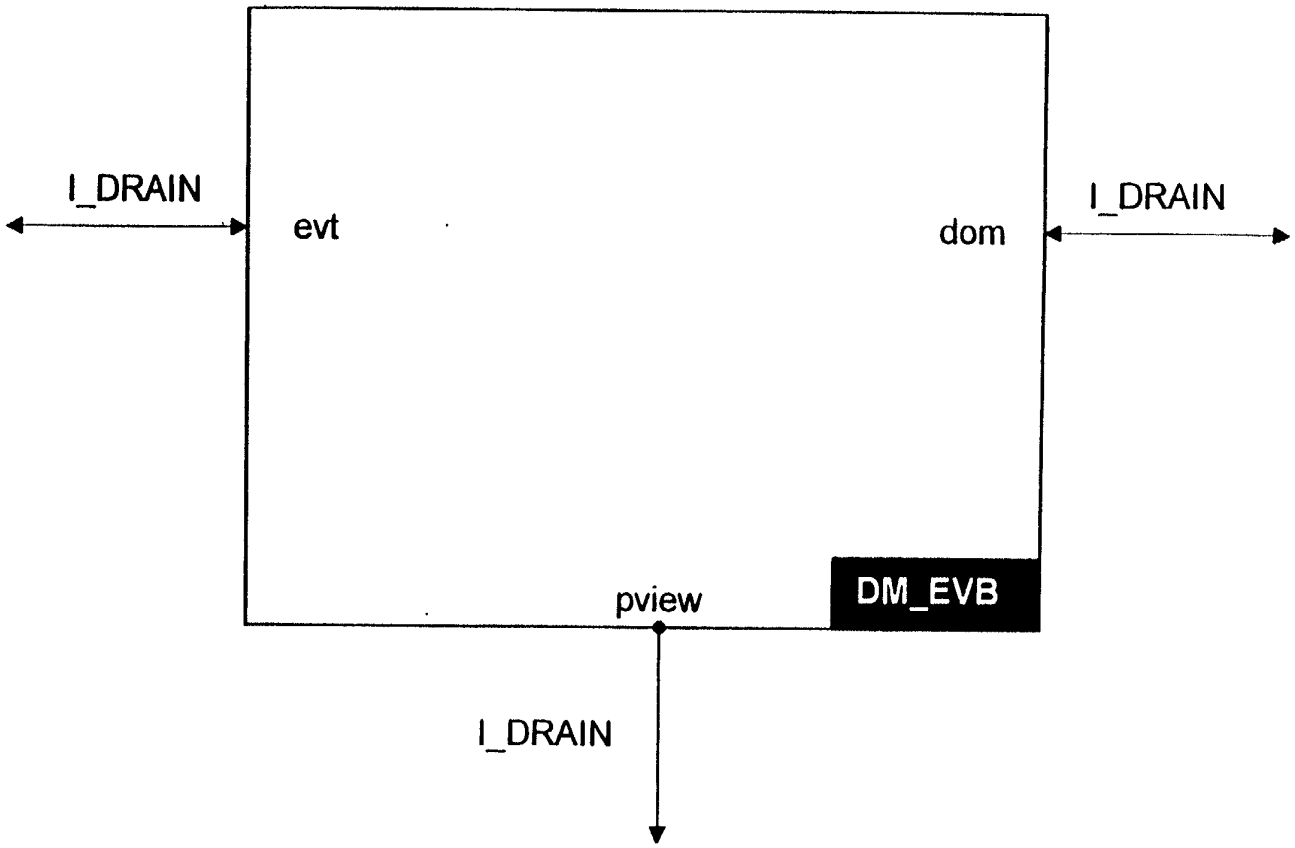


Fig. 33

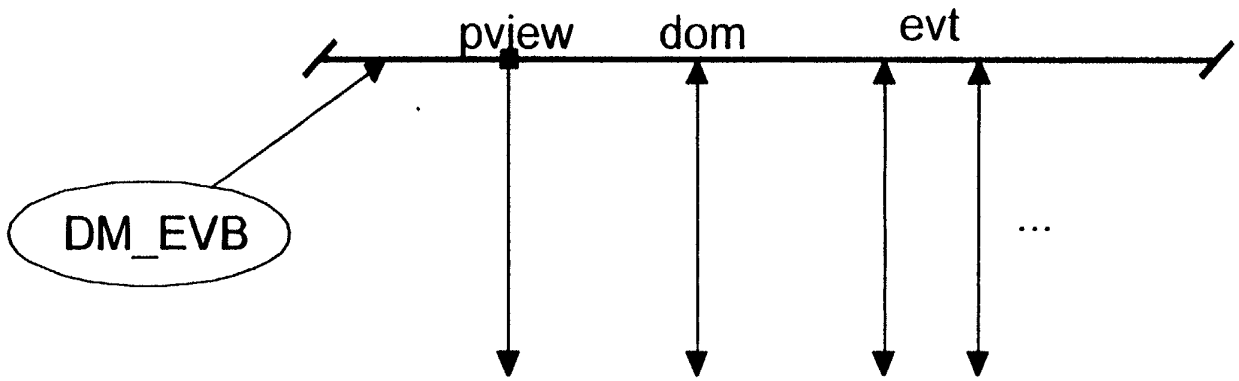
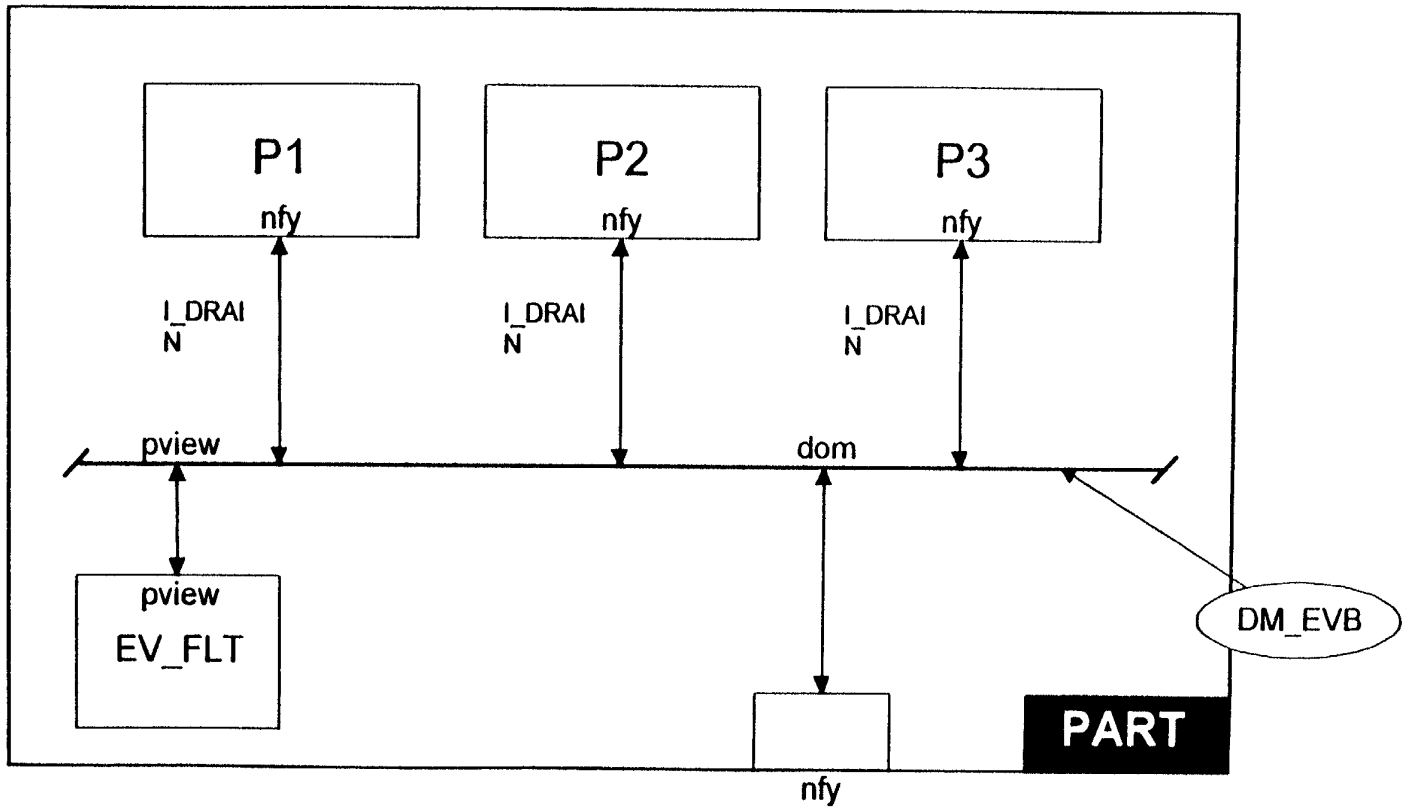


Fig. 34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P3
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EV_FLT
DM_EVB
PART
nfy

Fig. 35

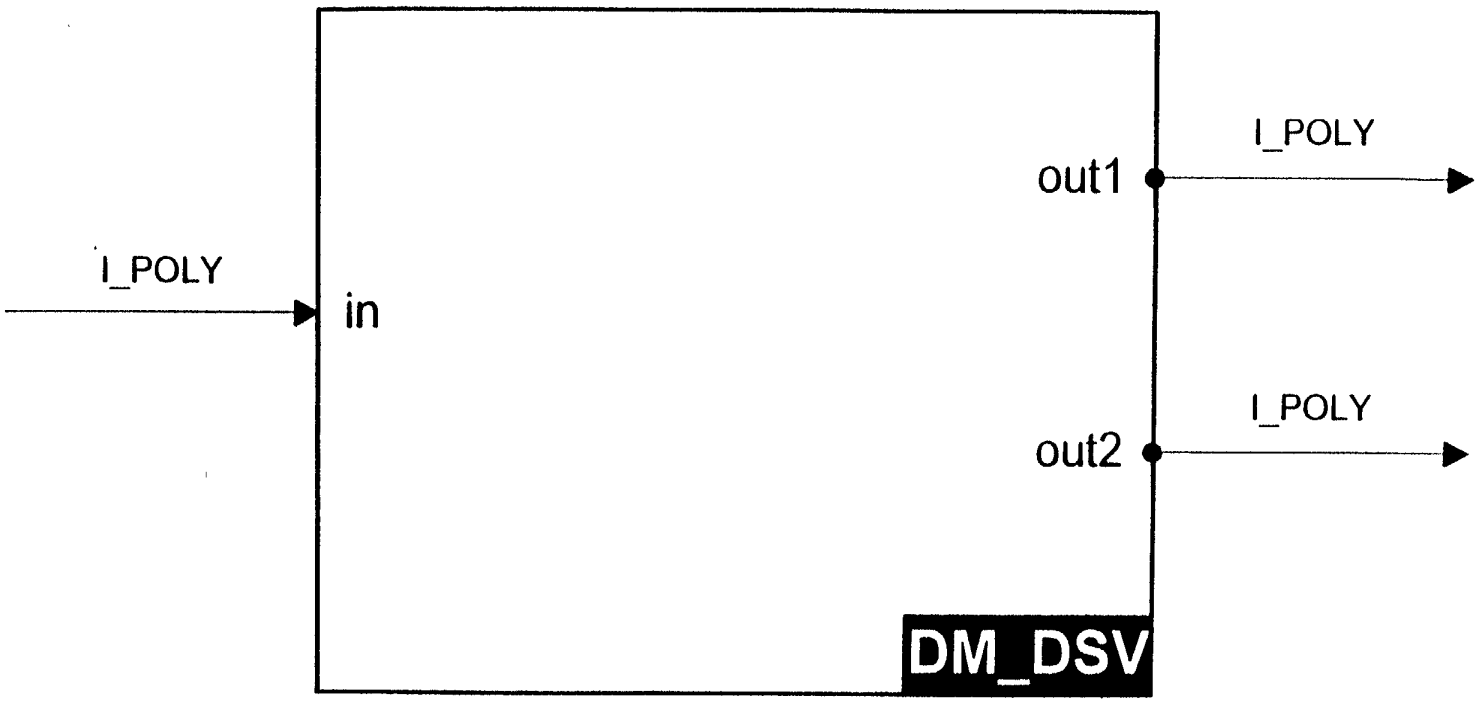
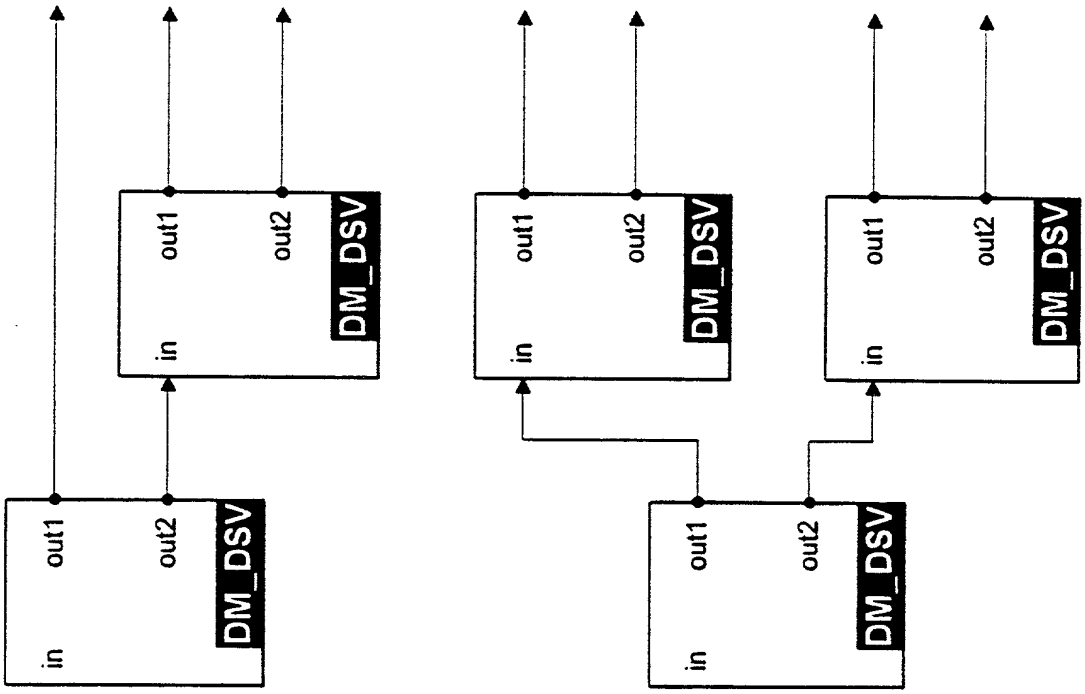


Fig. 36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out1
out2
DM_DSV
in
out1
out2
DM_DSV
in
out1
out2
DM_DSV

Fig. 37

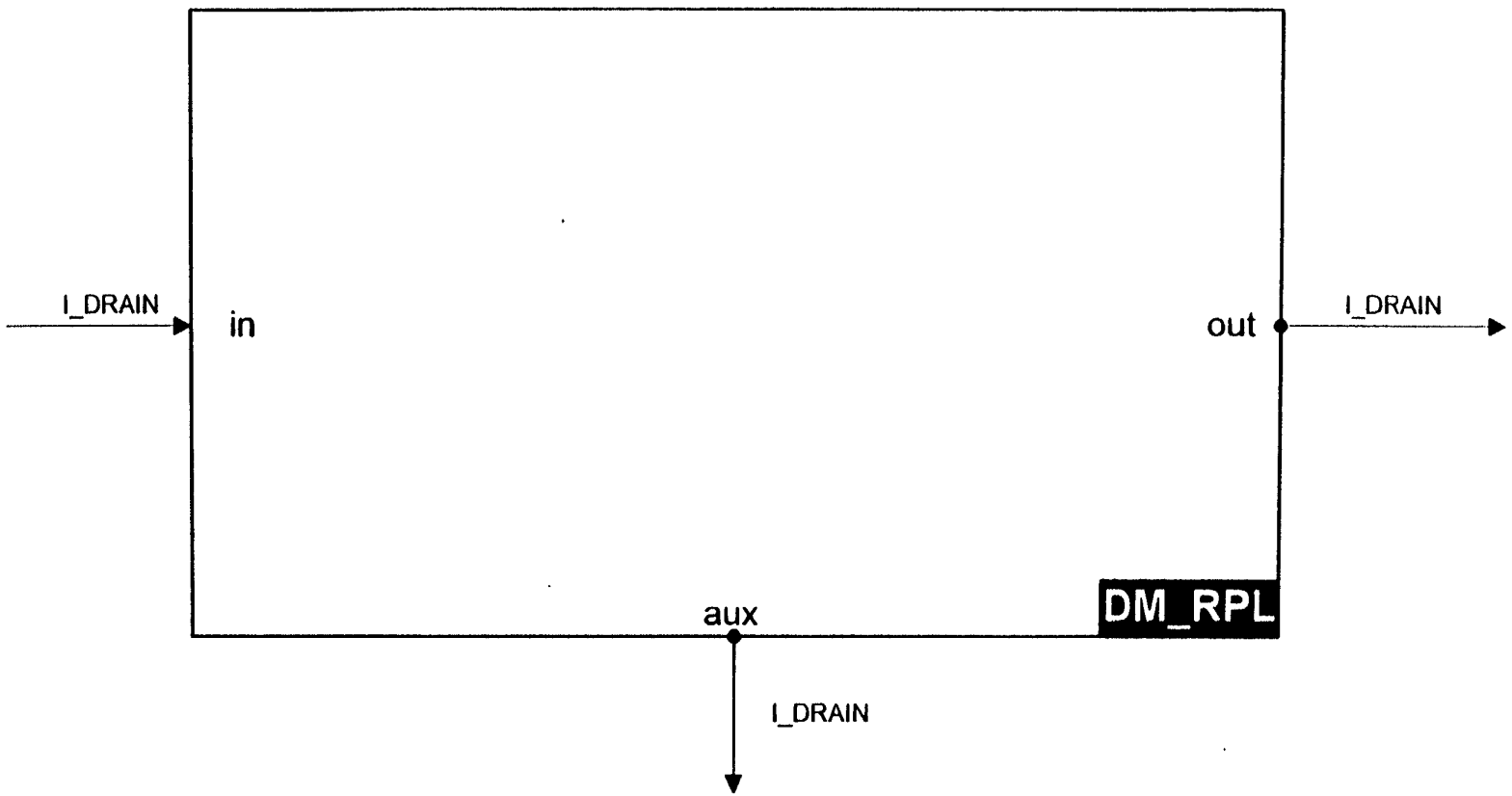


Fig. 38

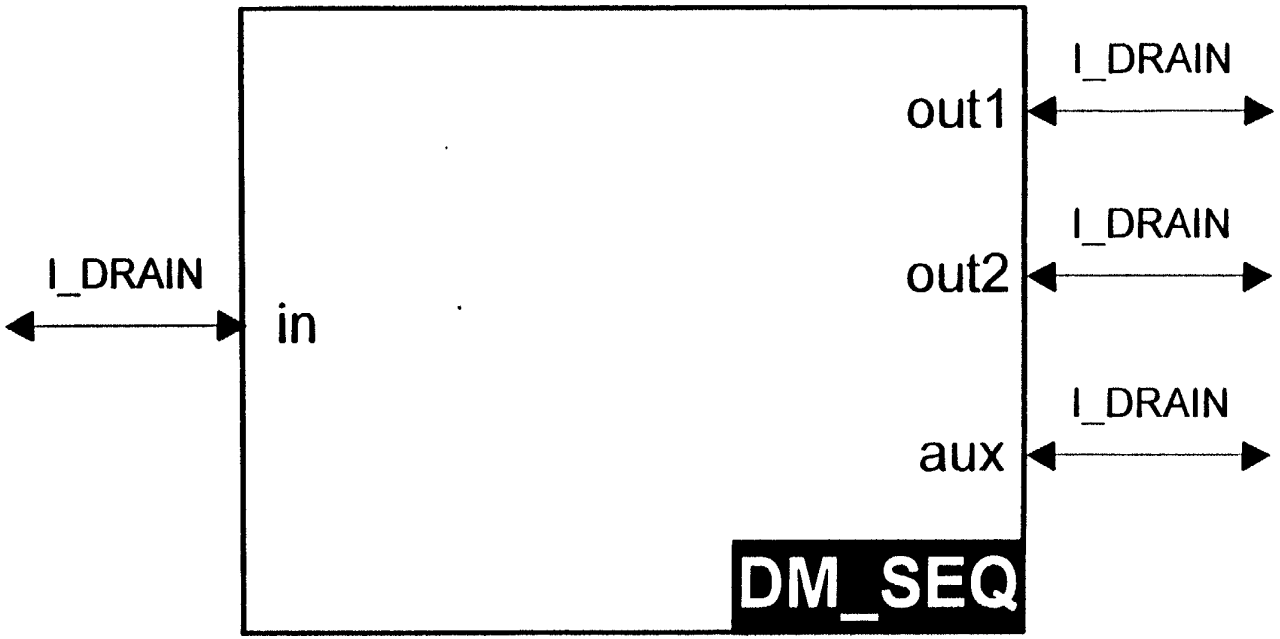


Fig. 39

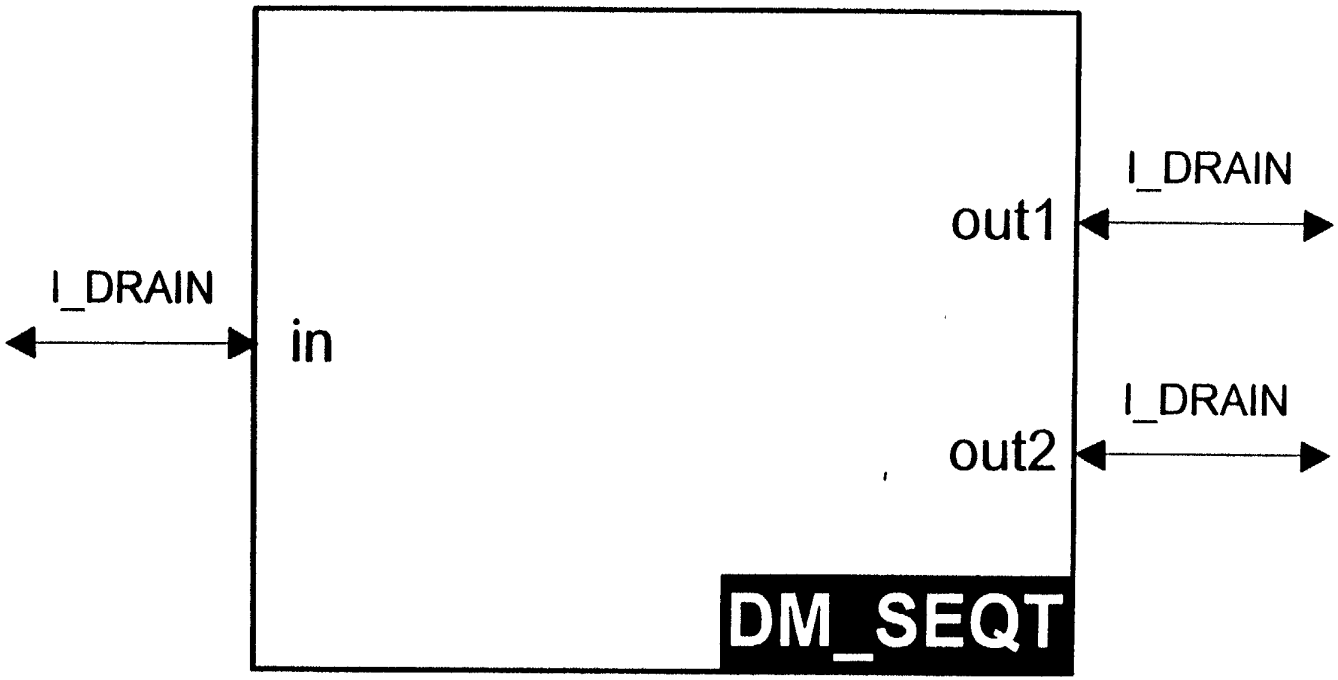
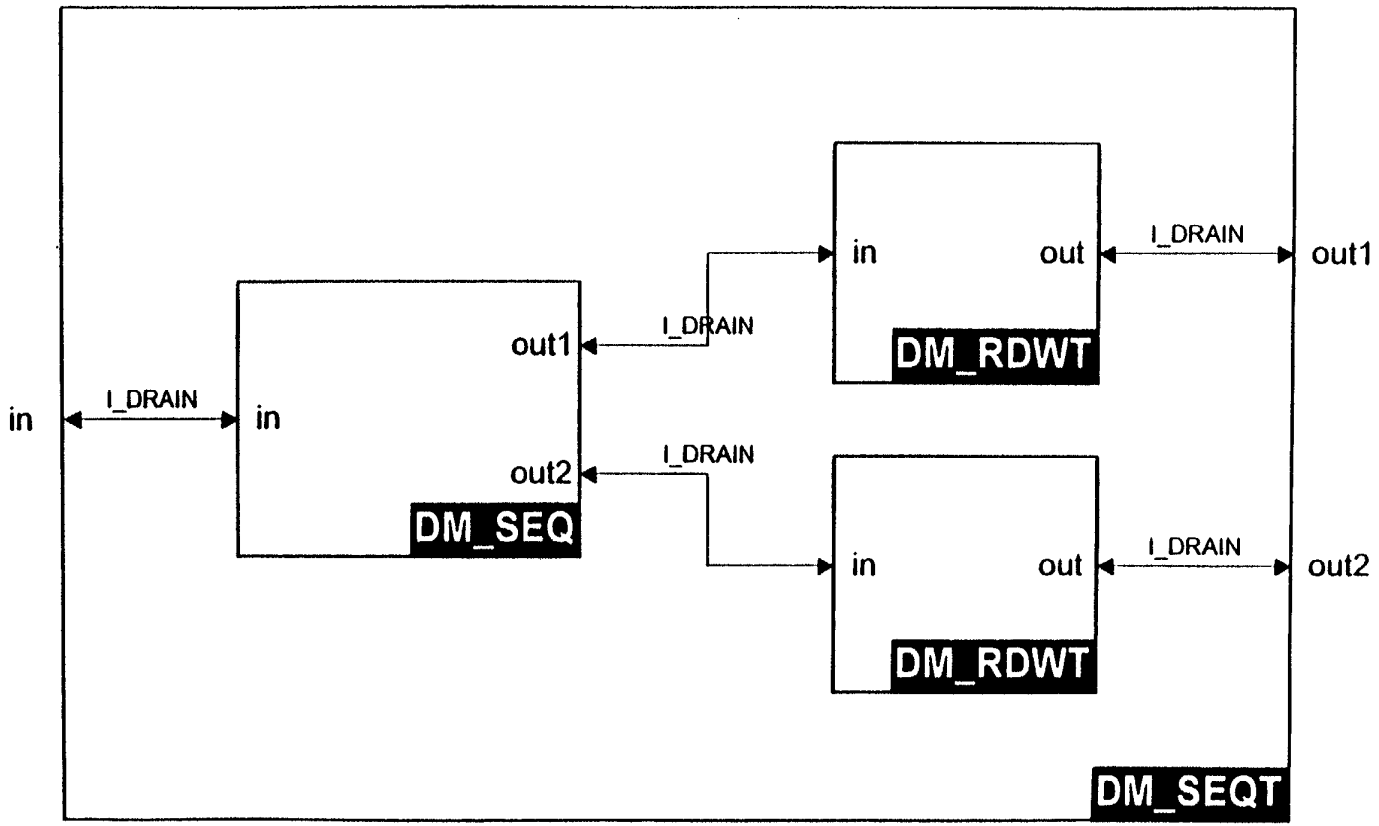


Fig. 40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out1
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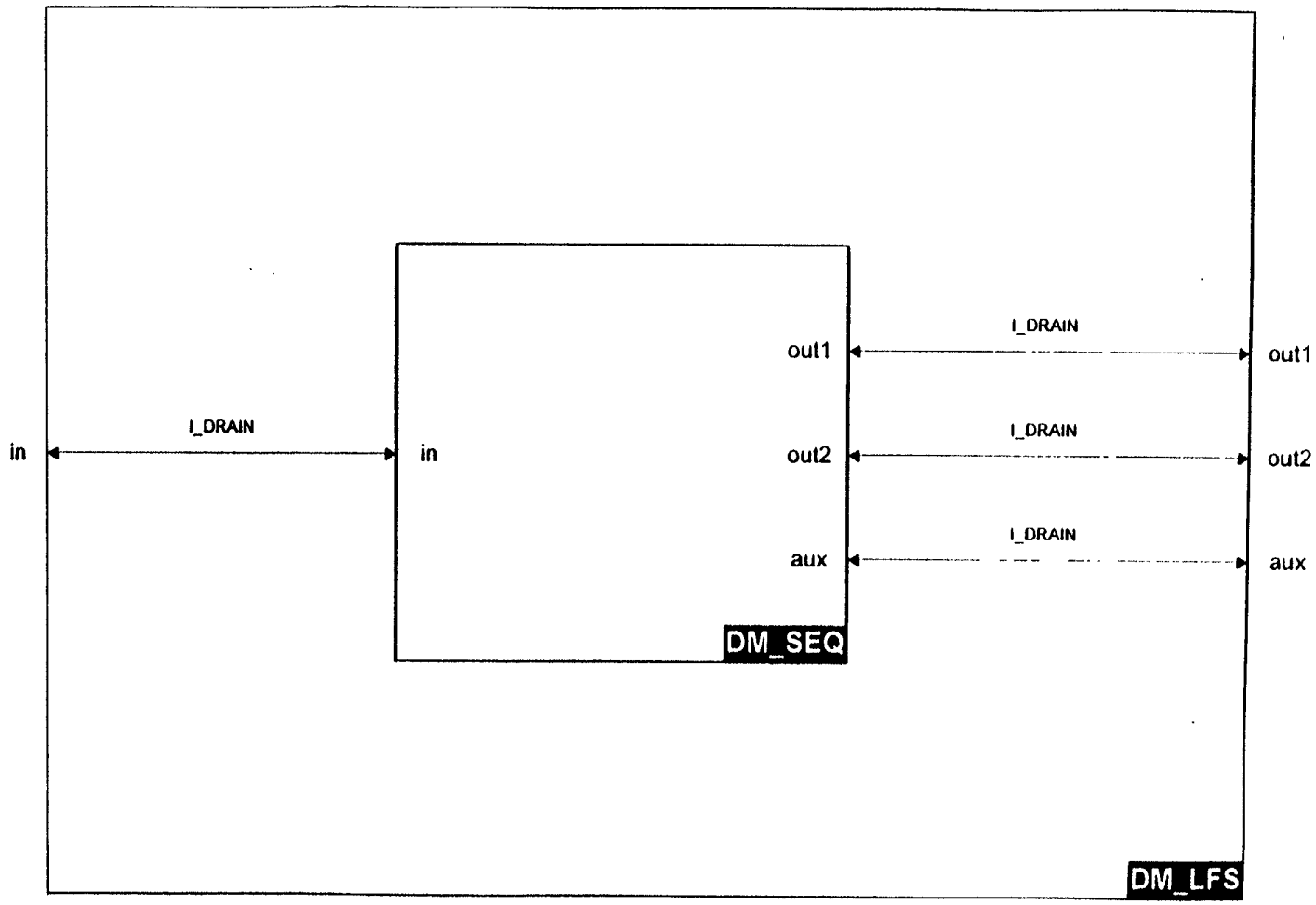
out2
DM_SEQT

Fig. 41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out1
out2
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DM_LFS

Fig. 42

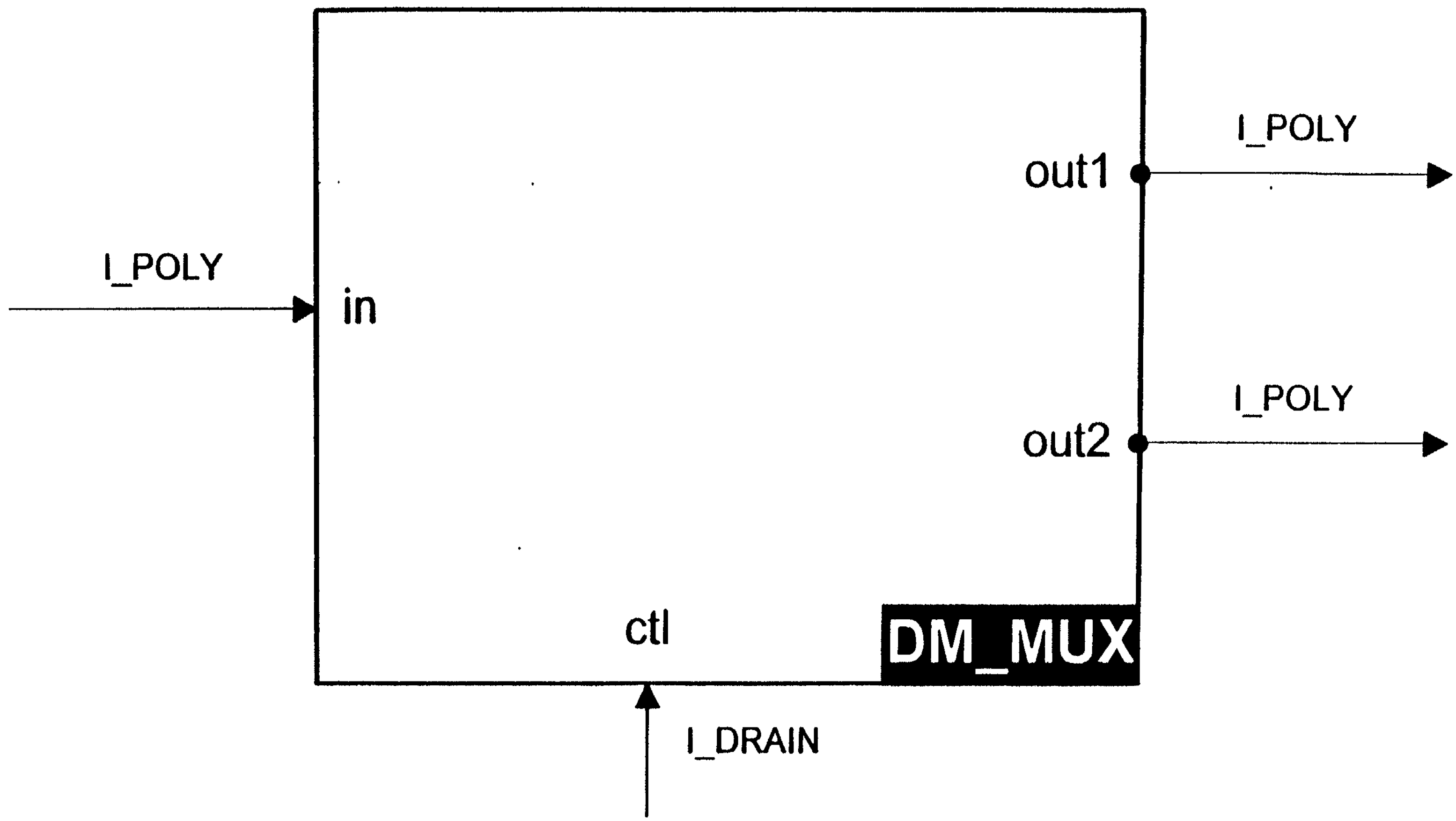


Fig. 43

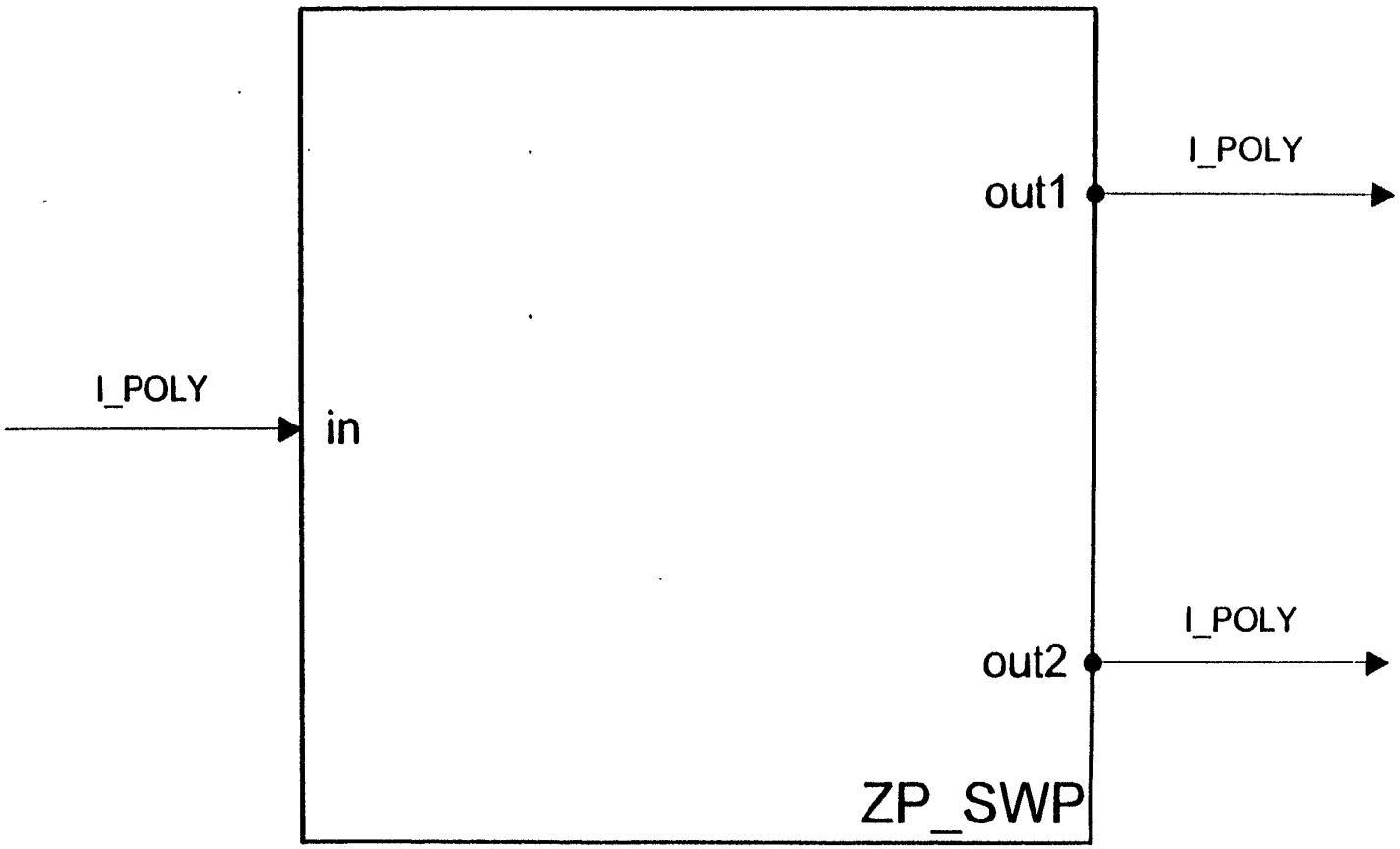


Fig. 44

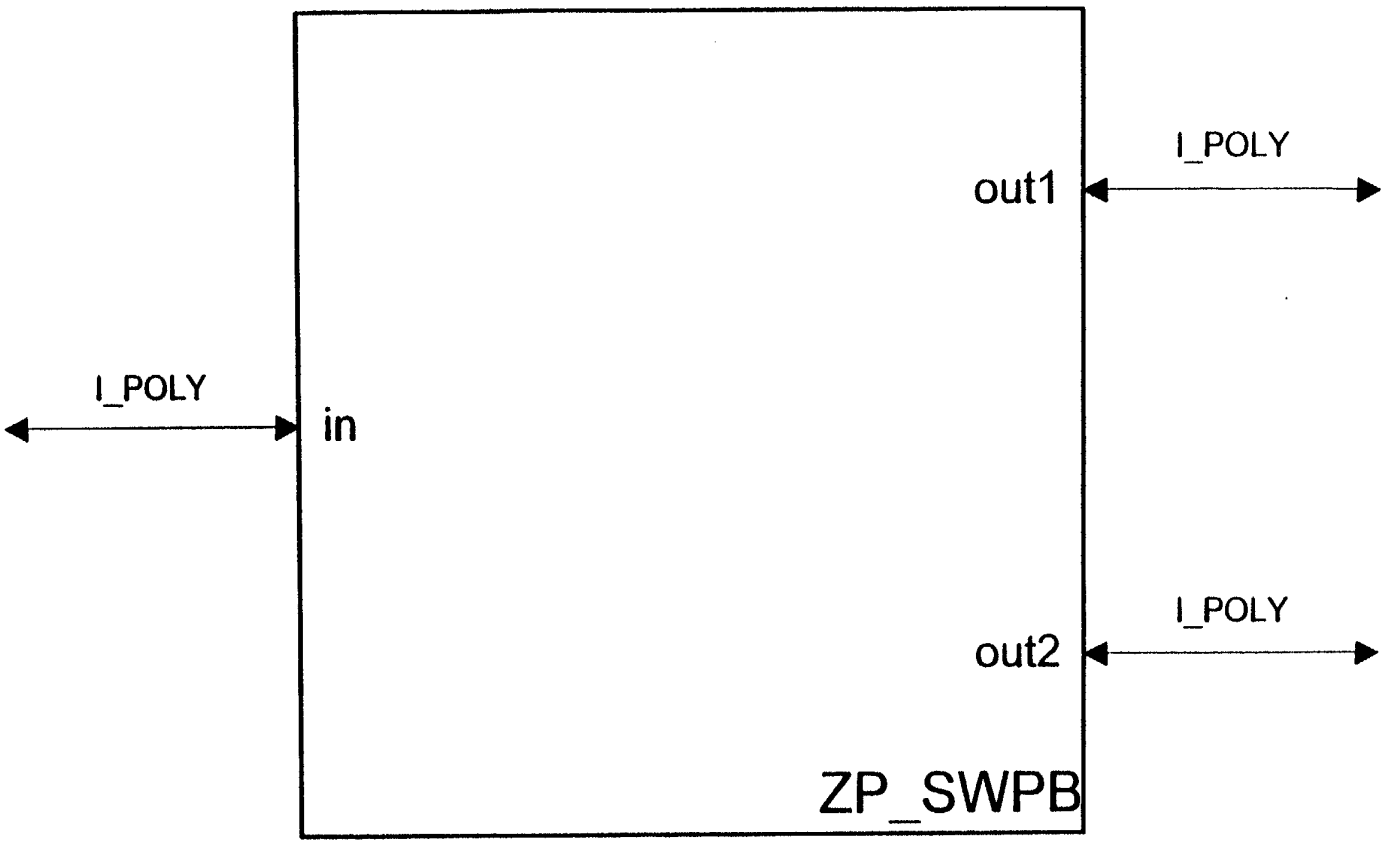


Fig. 45

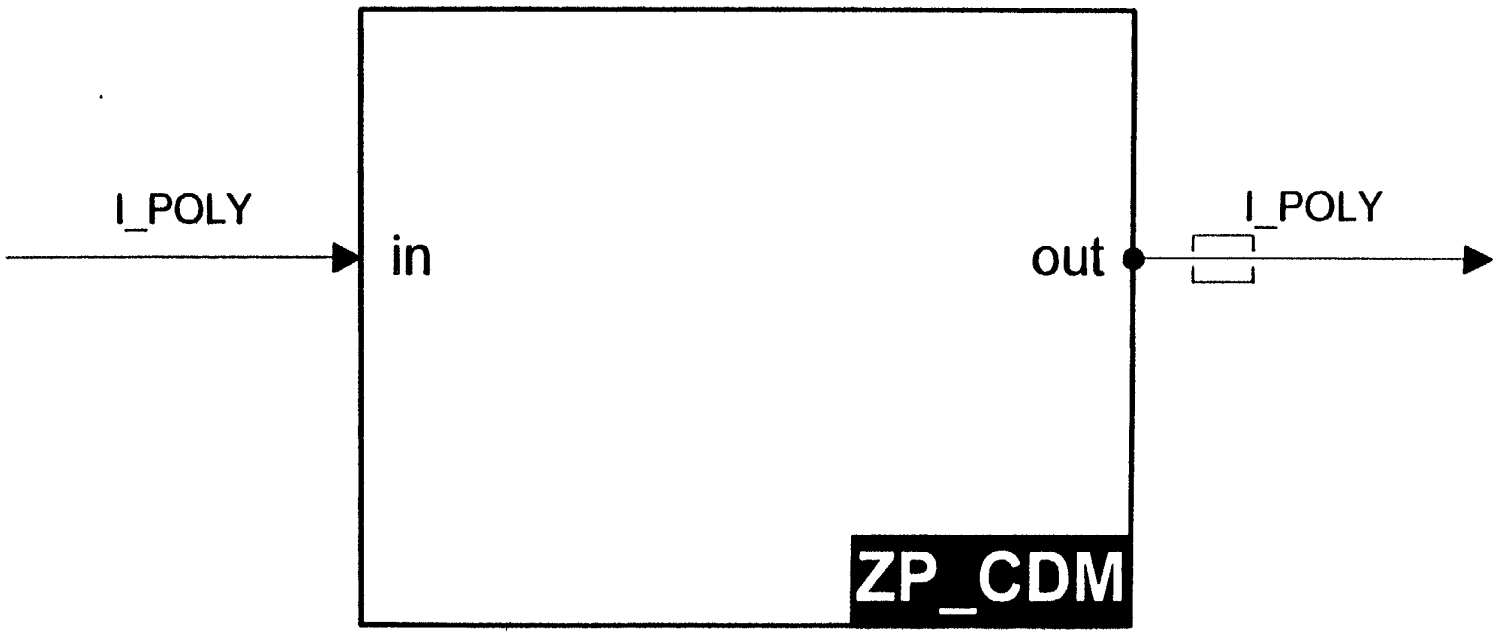


Fig. 46

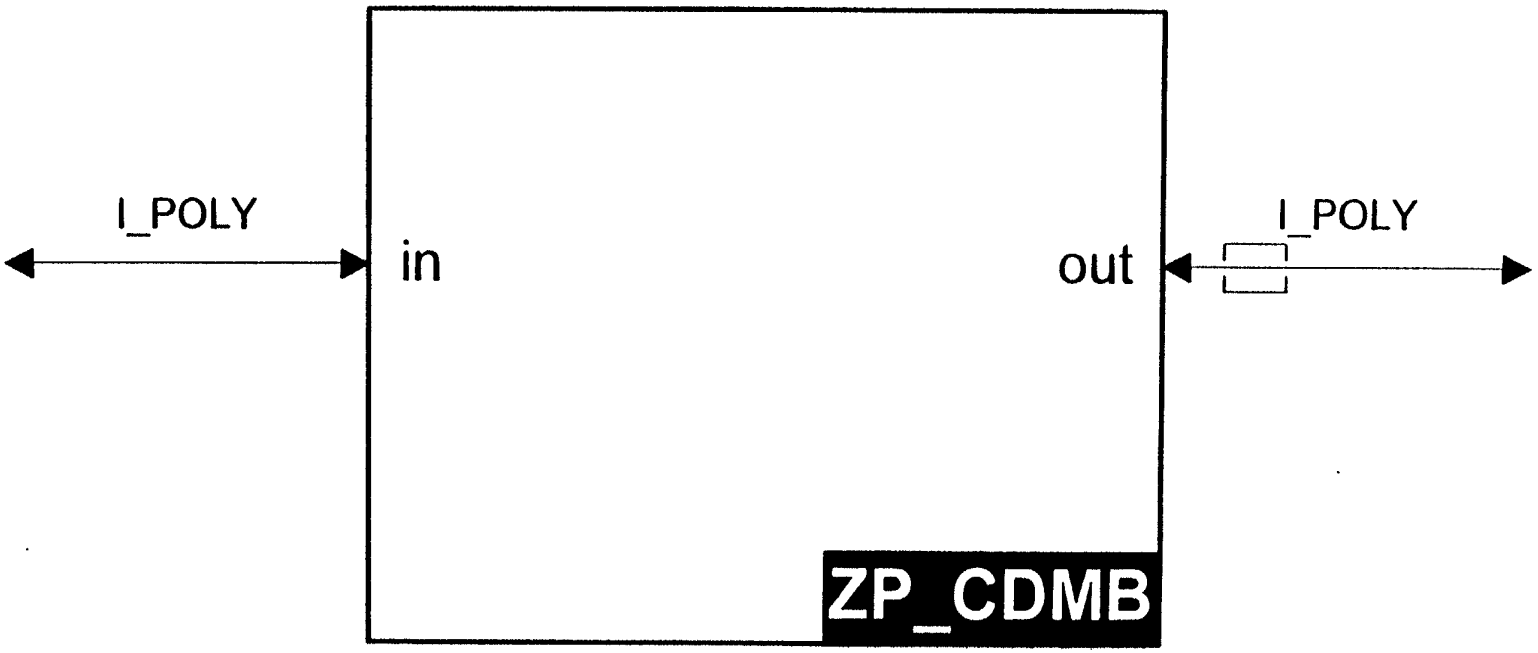


Fig. 47

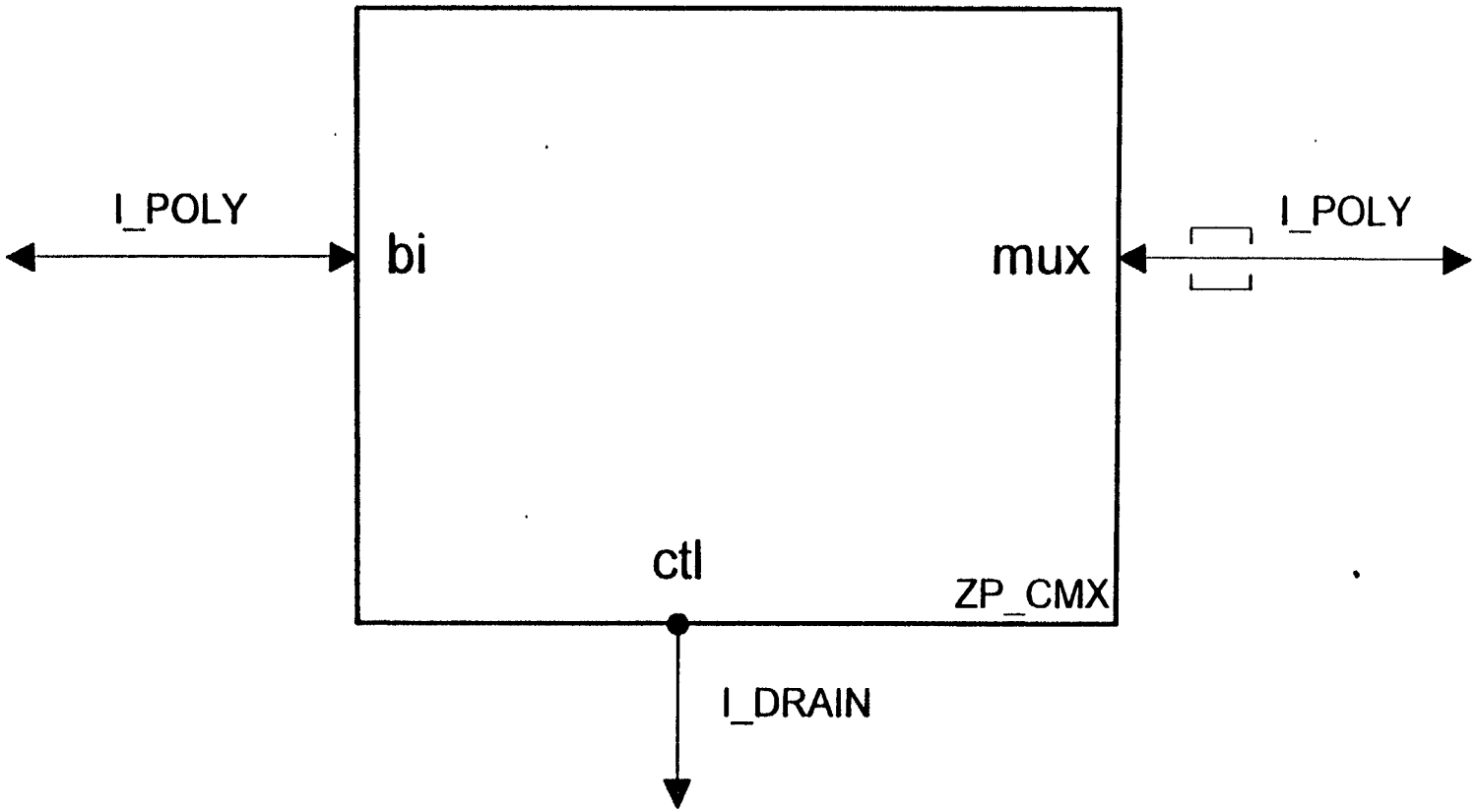


Fig. 48

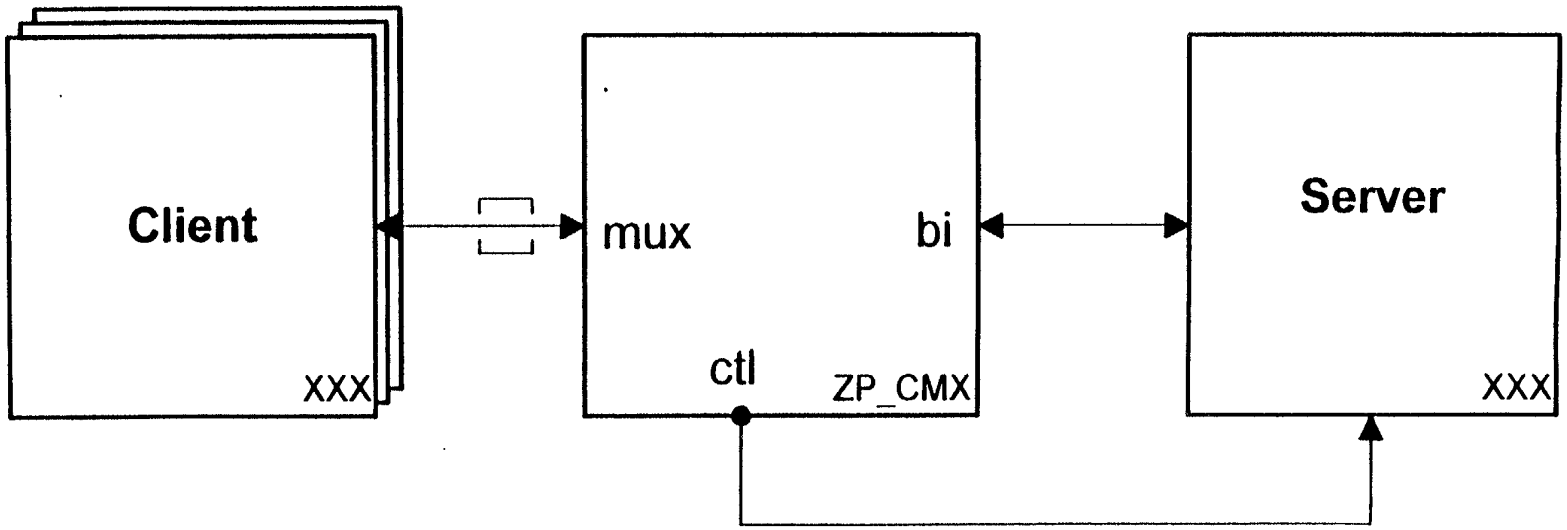
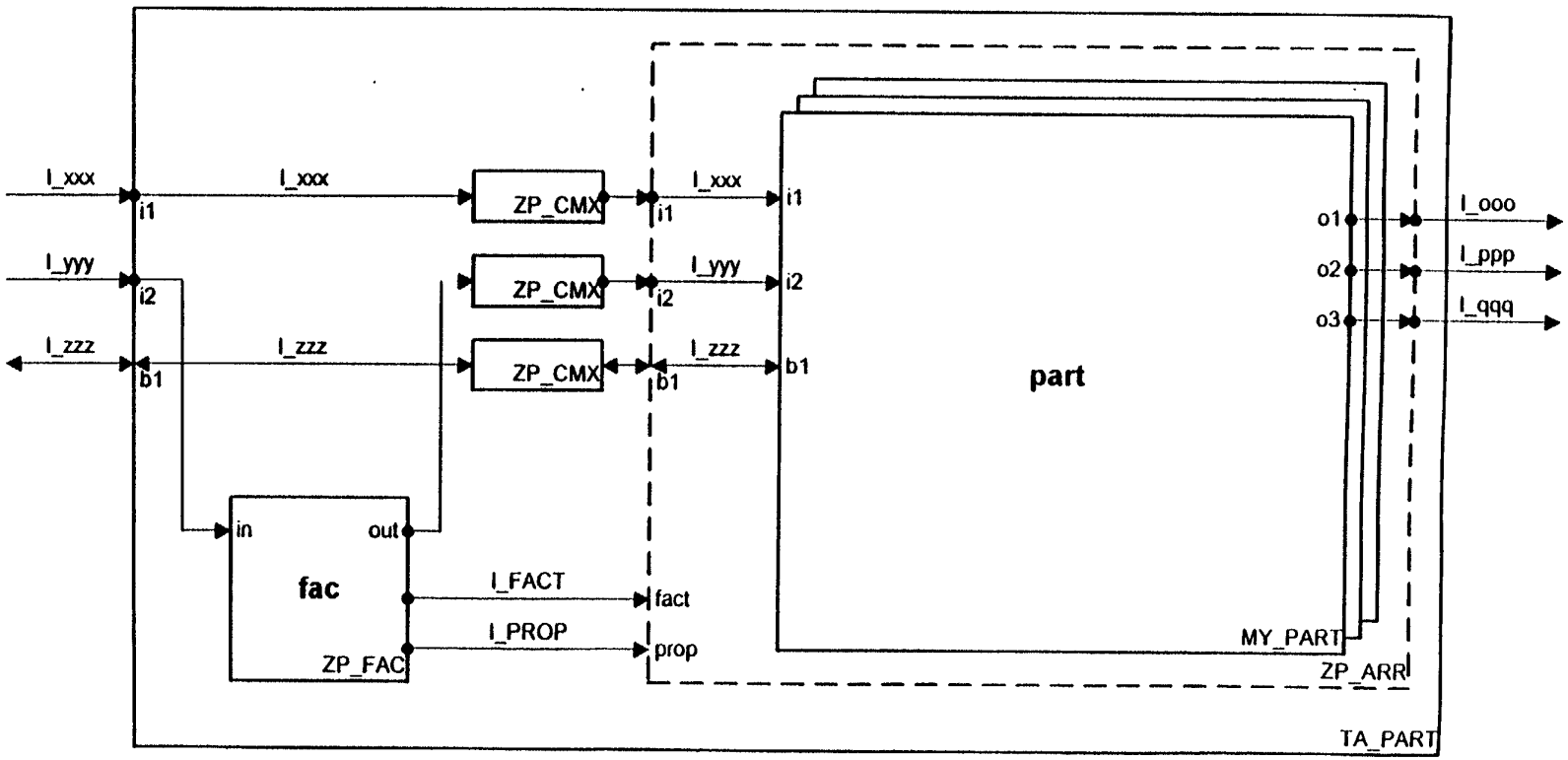


Fig. 49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b1
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b1
in
out
fac
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fact
I_PROP
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part
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o3
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I_qqq
MY_PART
ZP_ARR
TA_PART

Fig. 50

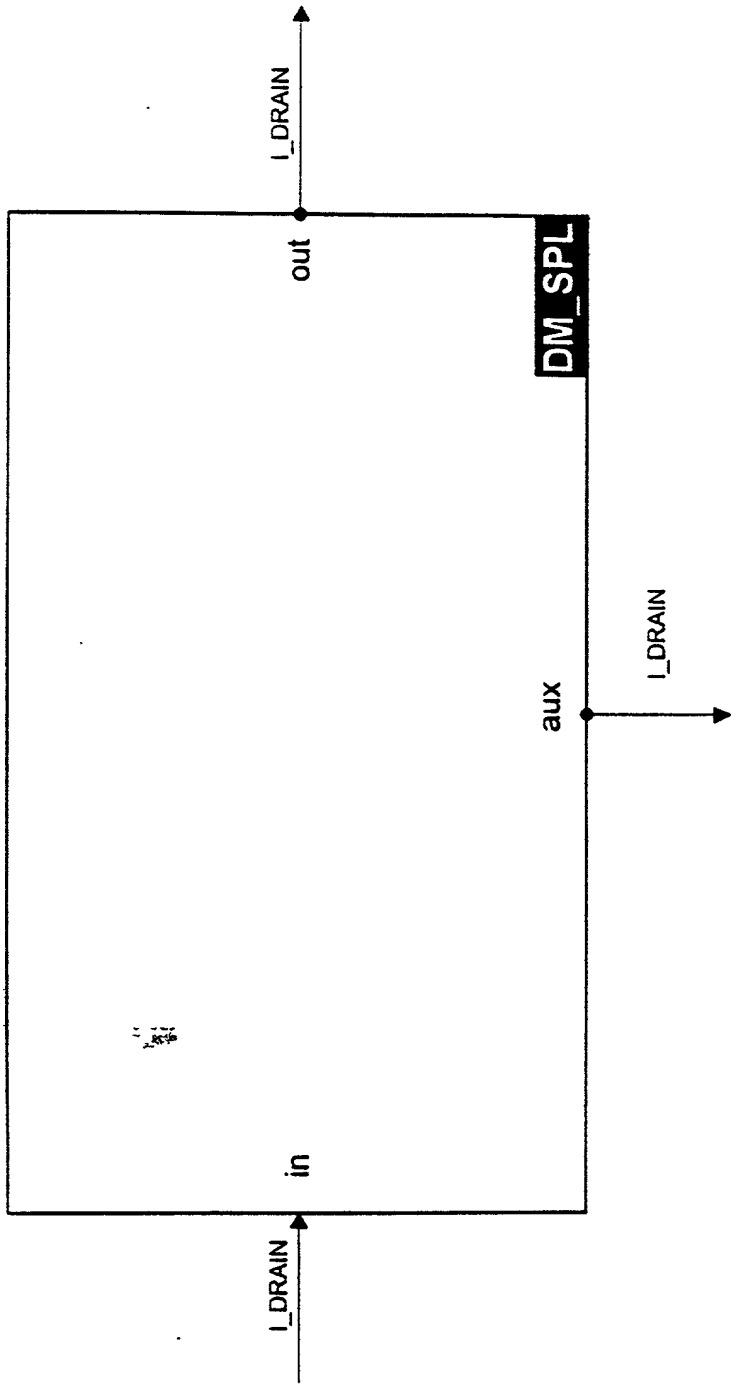


Fig. 51

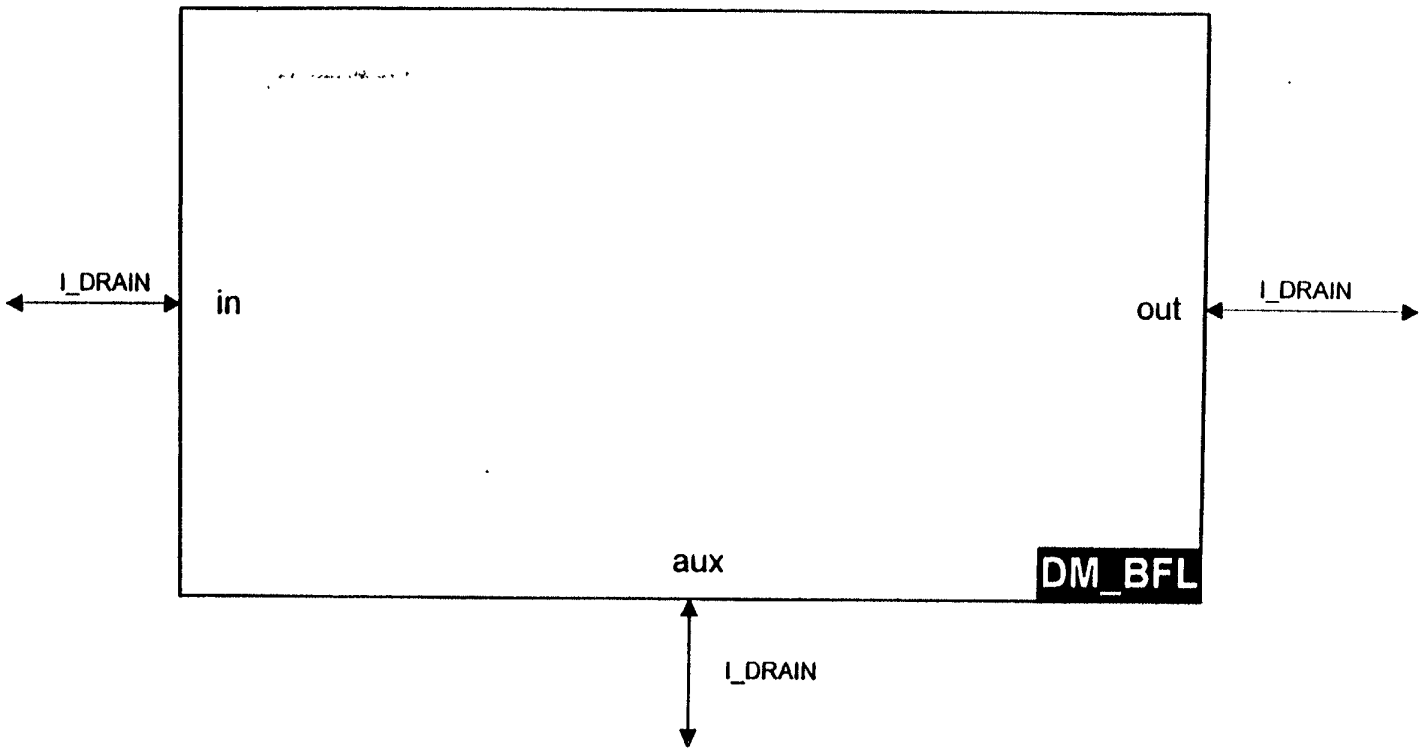
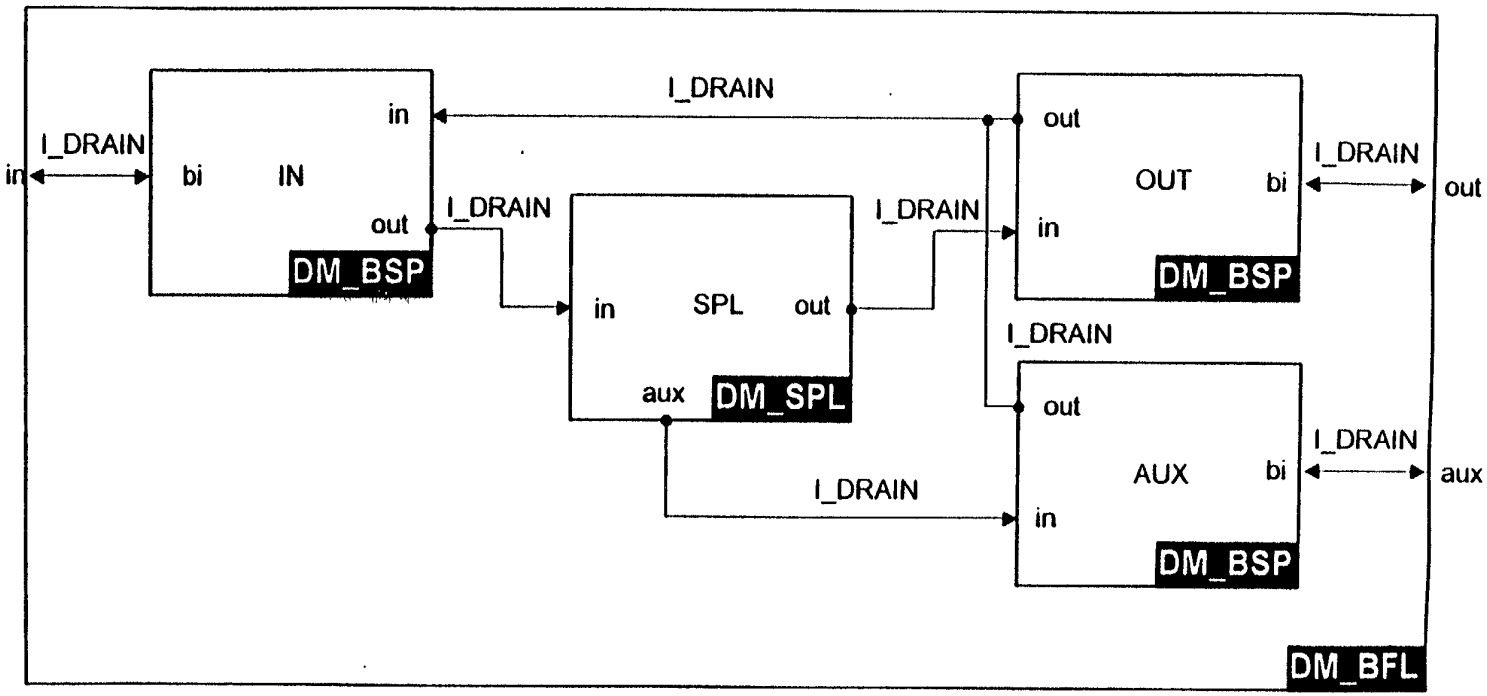


Fig. 52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aux
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out
OUT
bi
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AUX
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DM_BFL

Fig. 53

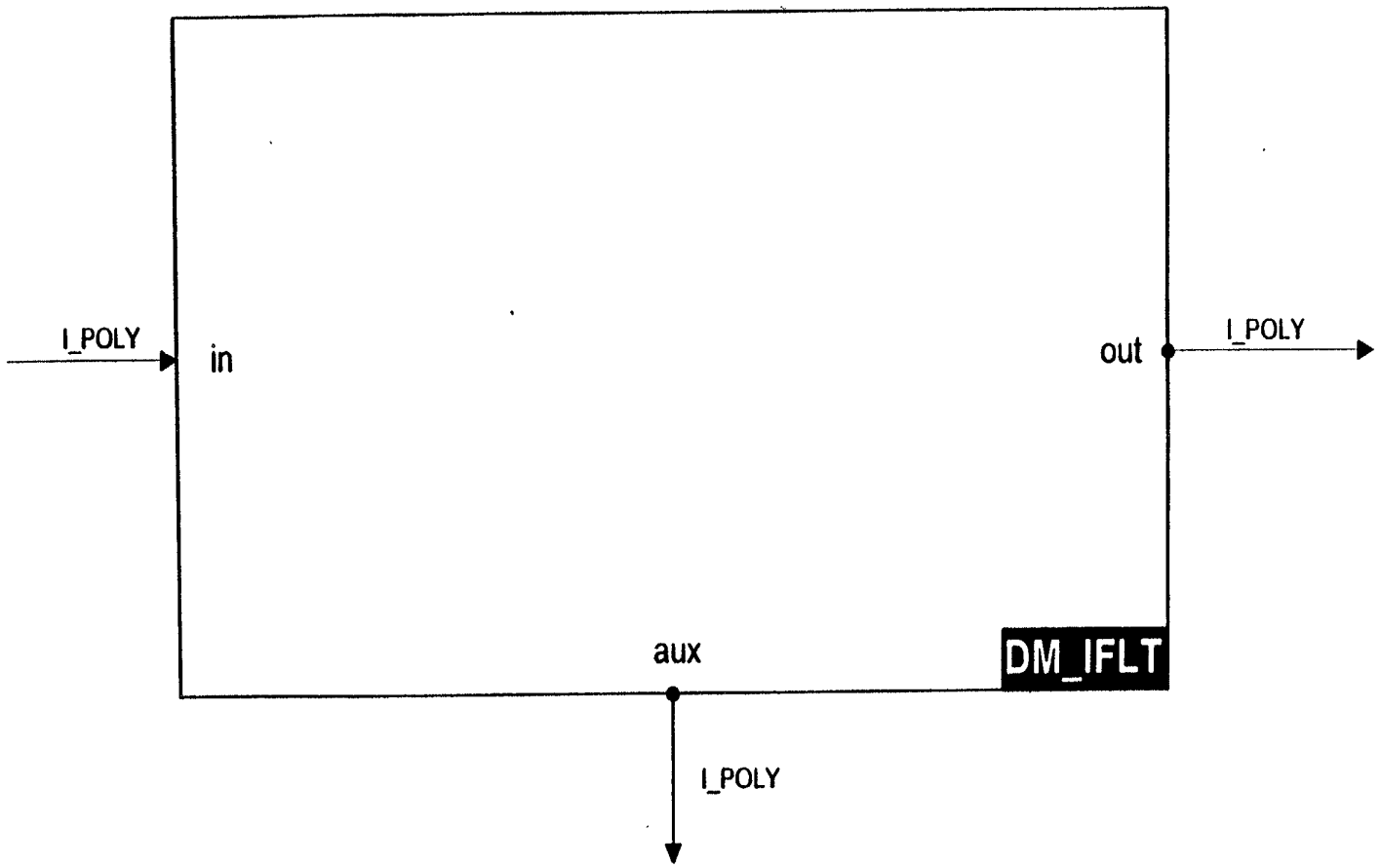


Fig. 54

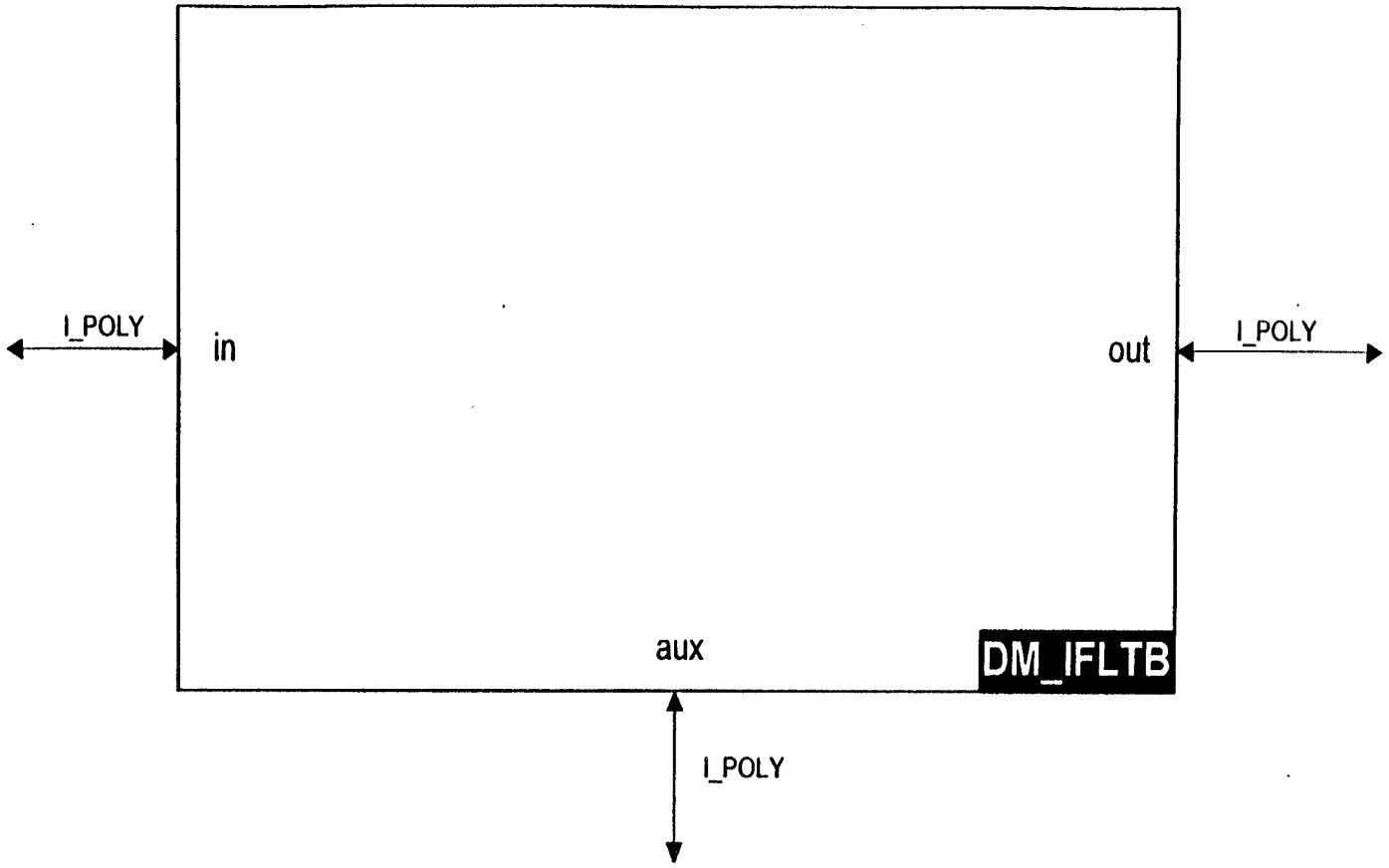


Fig. 55

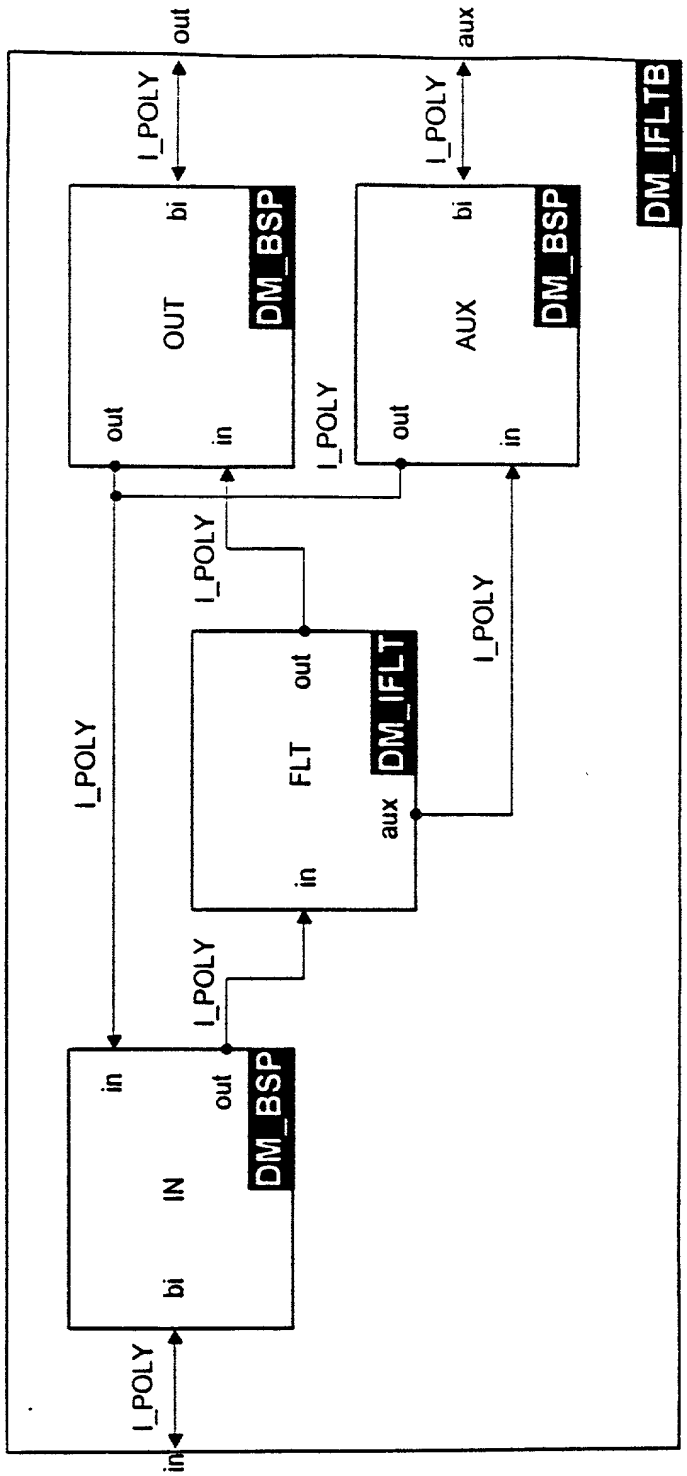

DM_IFLTB
out
aux
in
I_POLY
DM_BSP
OUT
bi
out
in
DM_BSP
AUX
bi
out
in
DM_IFLT
FLT
out
aux
in
DM_BSP
IN
in
out
bi

Fig. 56

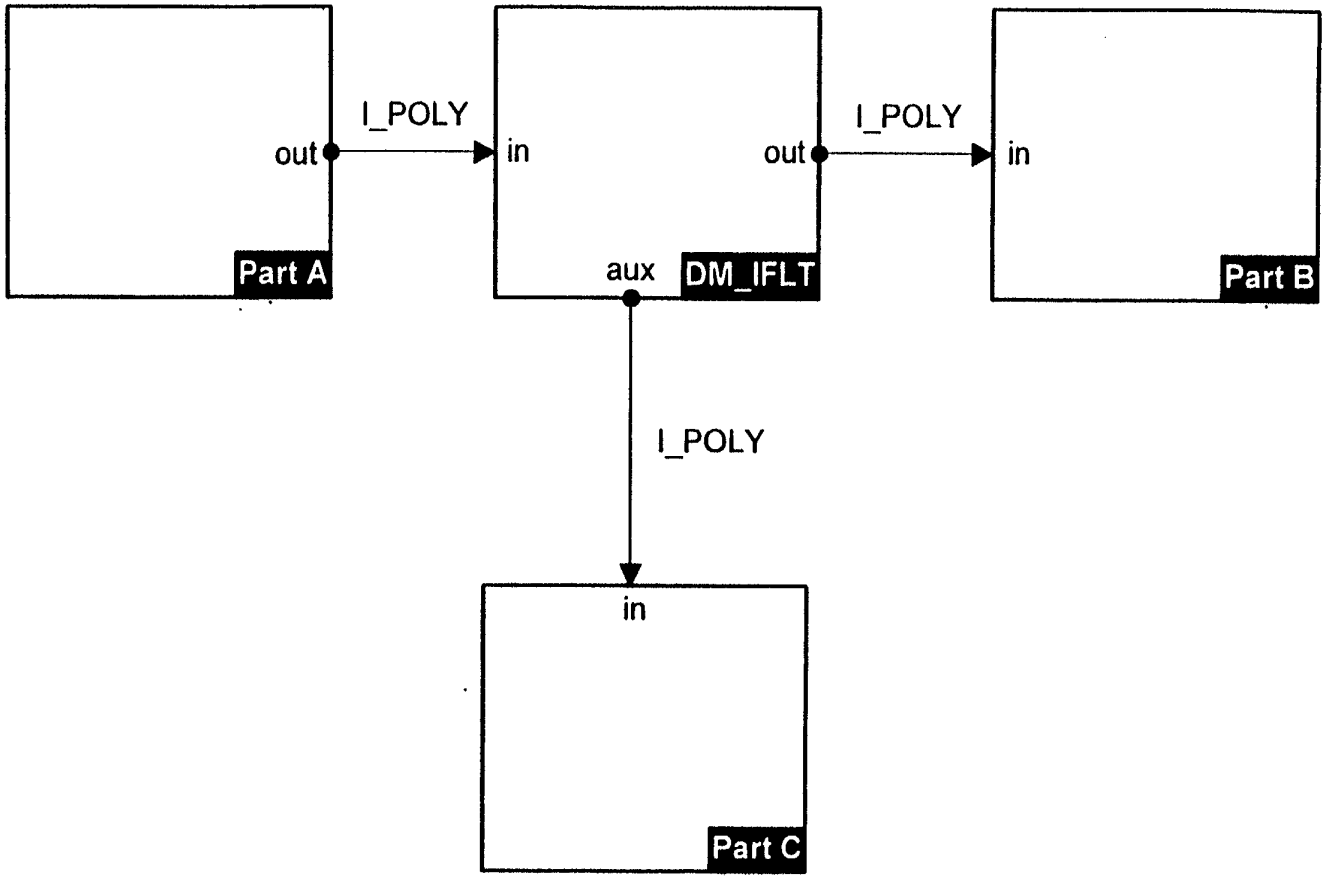


Fig. 57

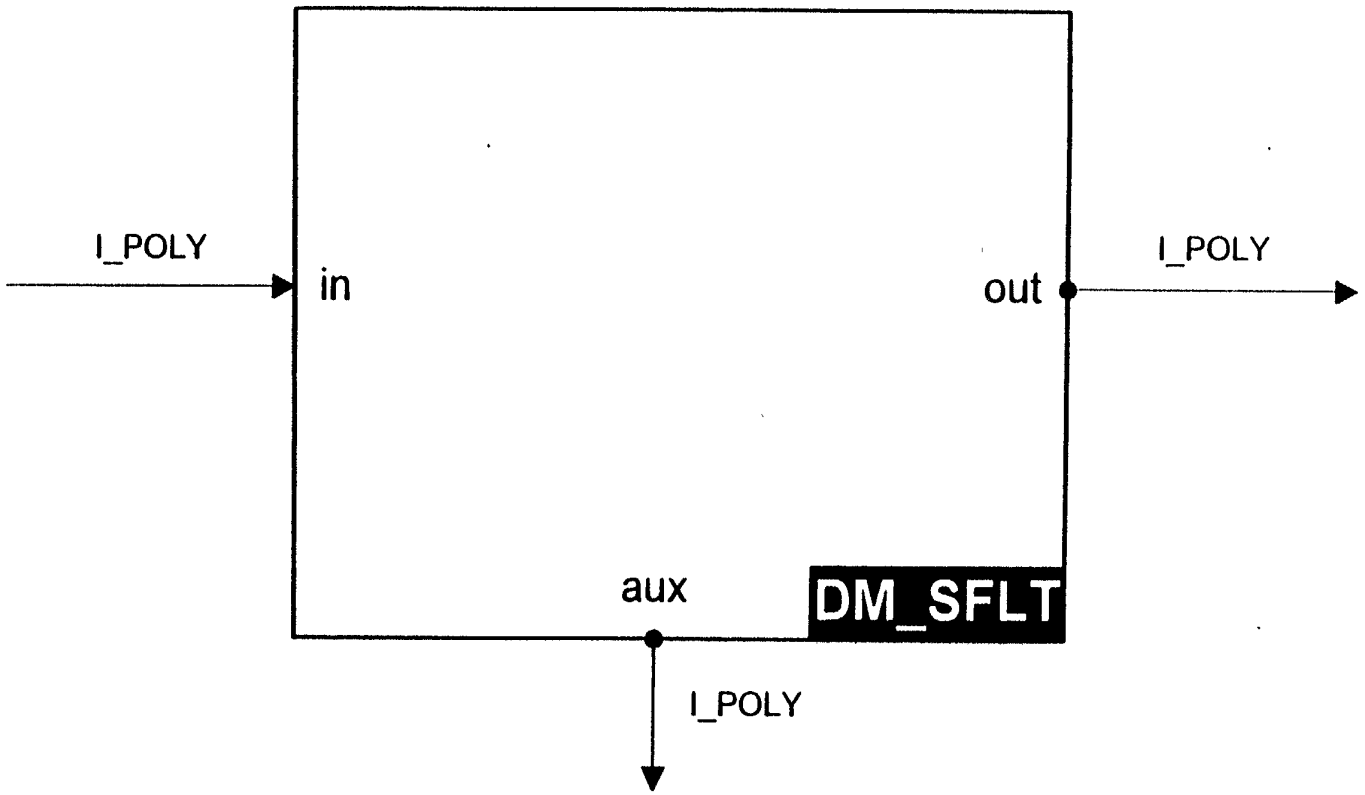


Fig. 58

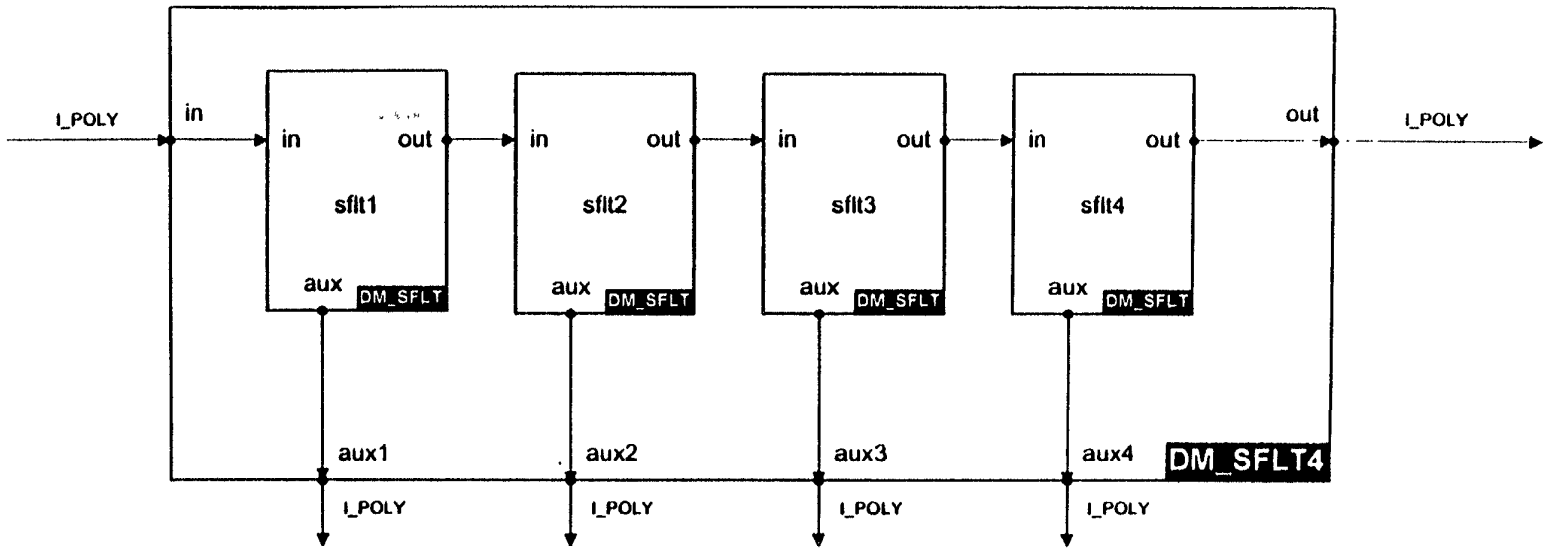

I_POLY
in
in
out
sflt1
aux
DM_SFLT
in
out
sflt2
aux
DM_SFLT
in
out
sflt3
aux
DM_SFLT
in
out
sflt4
aux
DM_SFLT
out
I_POLY
aux1
aux2
aux3
aux4
DM_SFLT4
I_POLY
I_POLY
I_POLY
I_POLY

Fig. 59

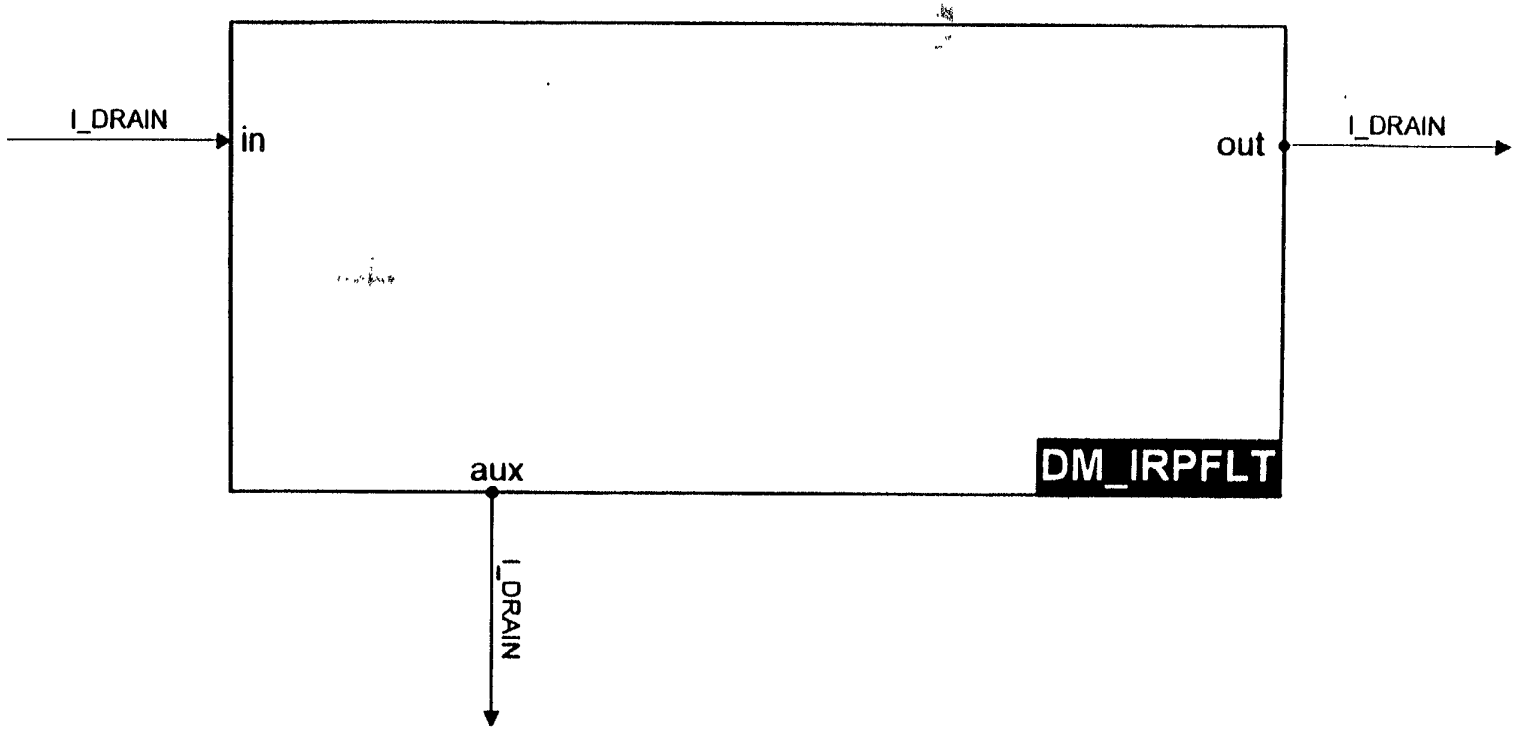


Fig. 60

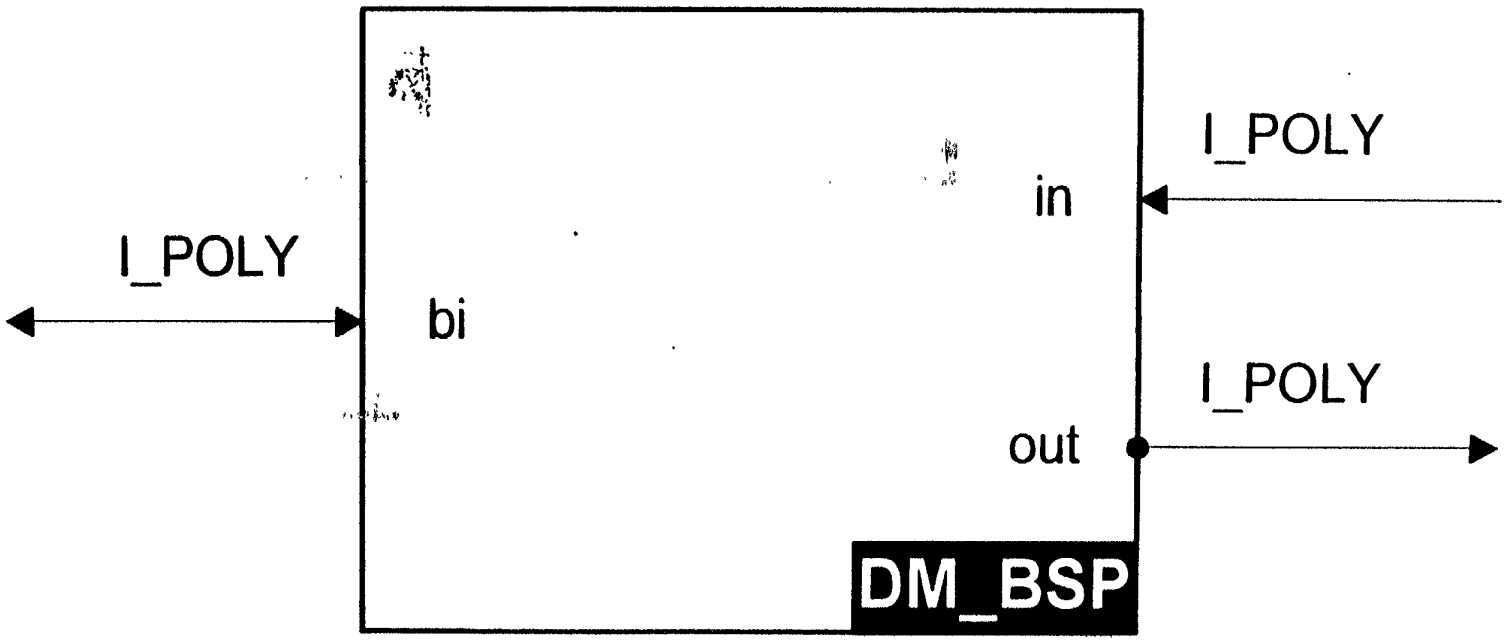


Fig. 61

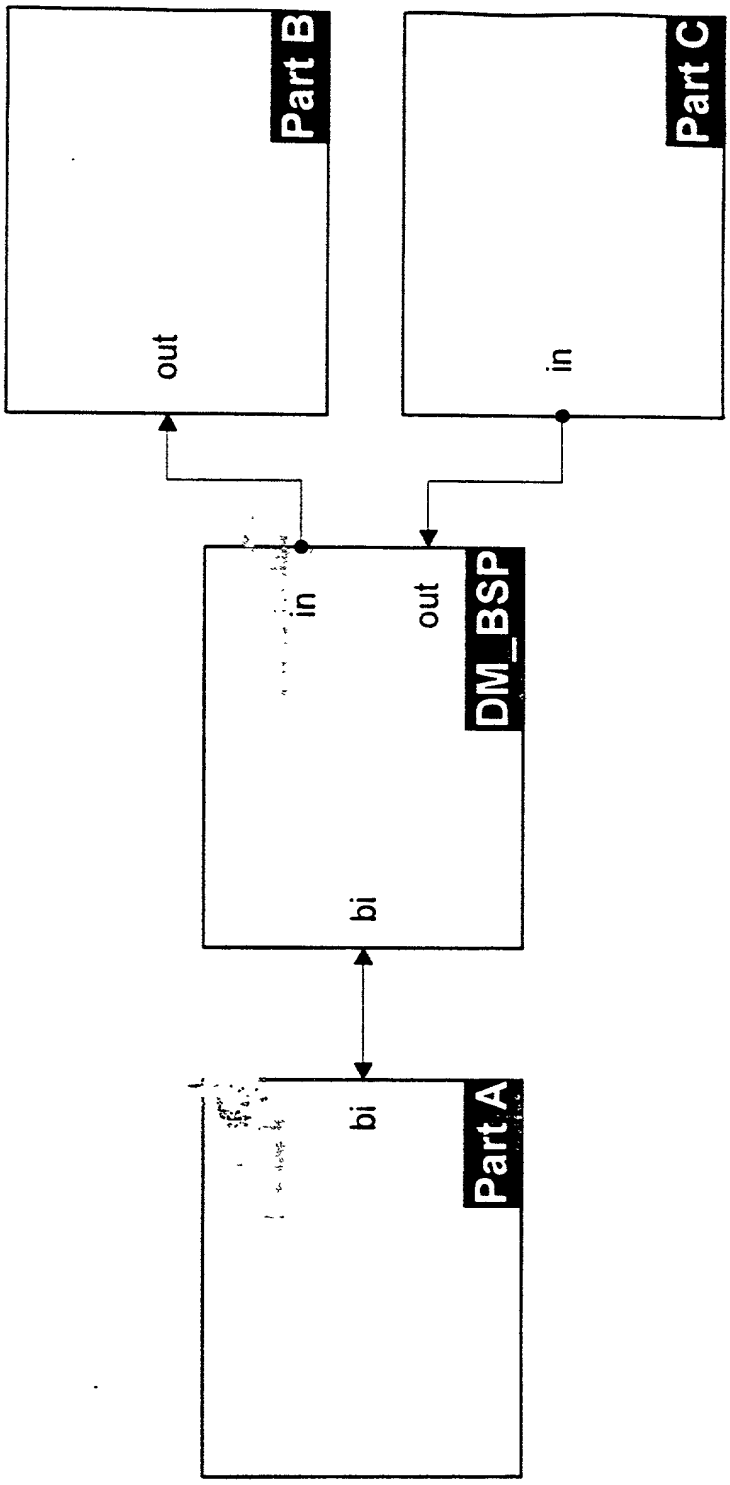


Fig. 62

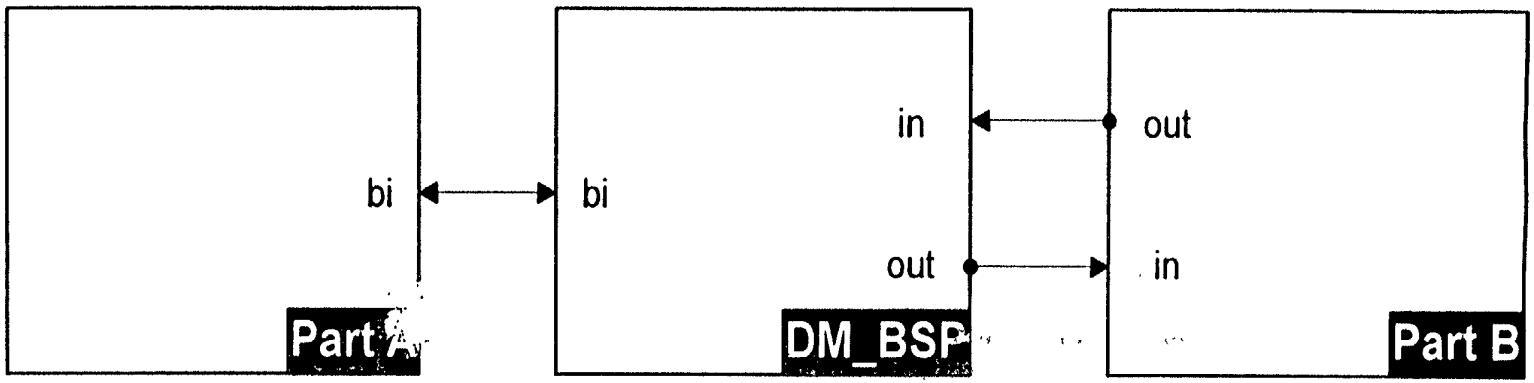


Fig. 63

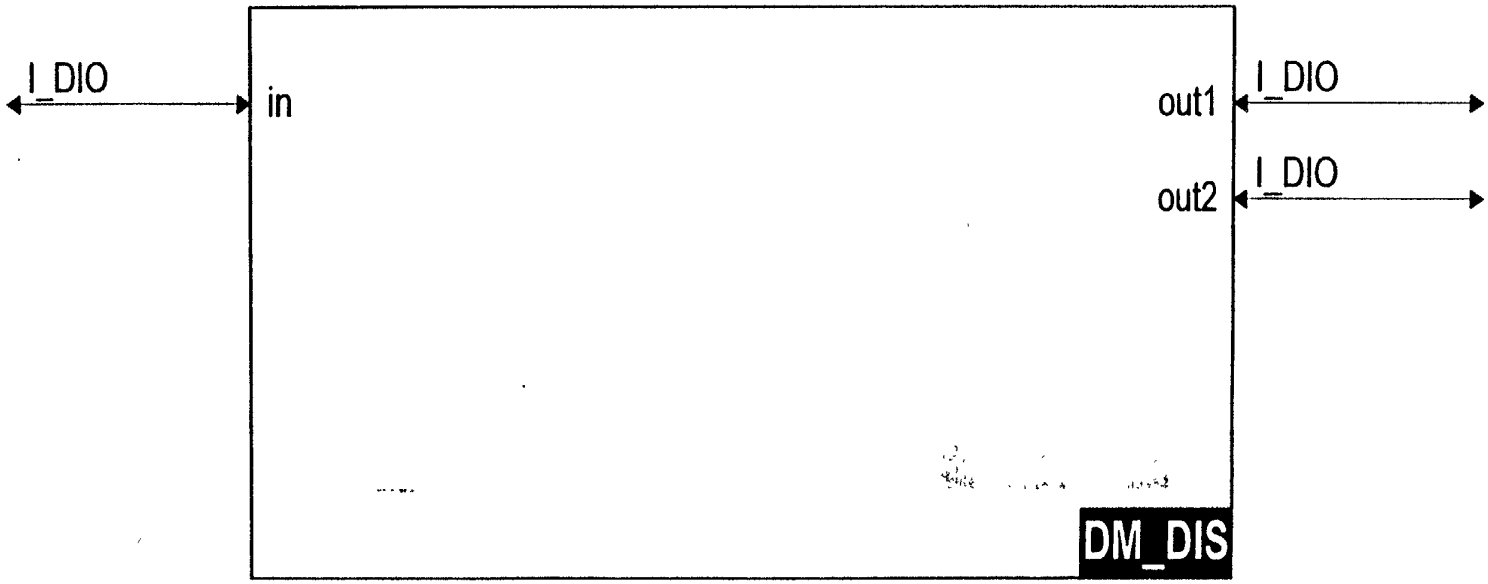


Fig. 64

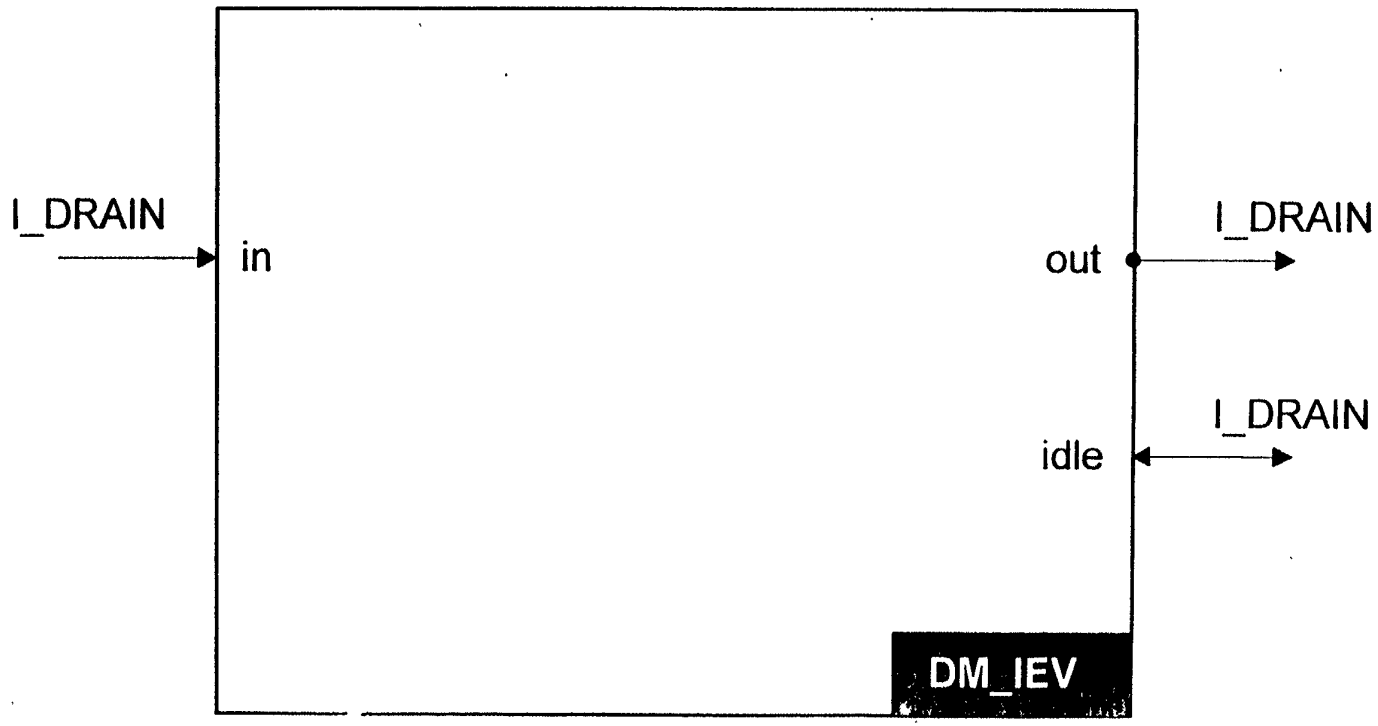


Fig. 65

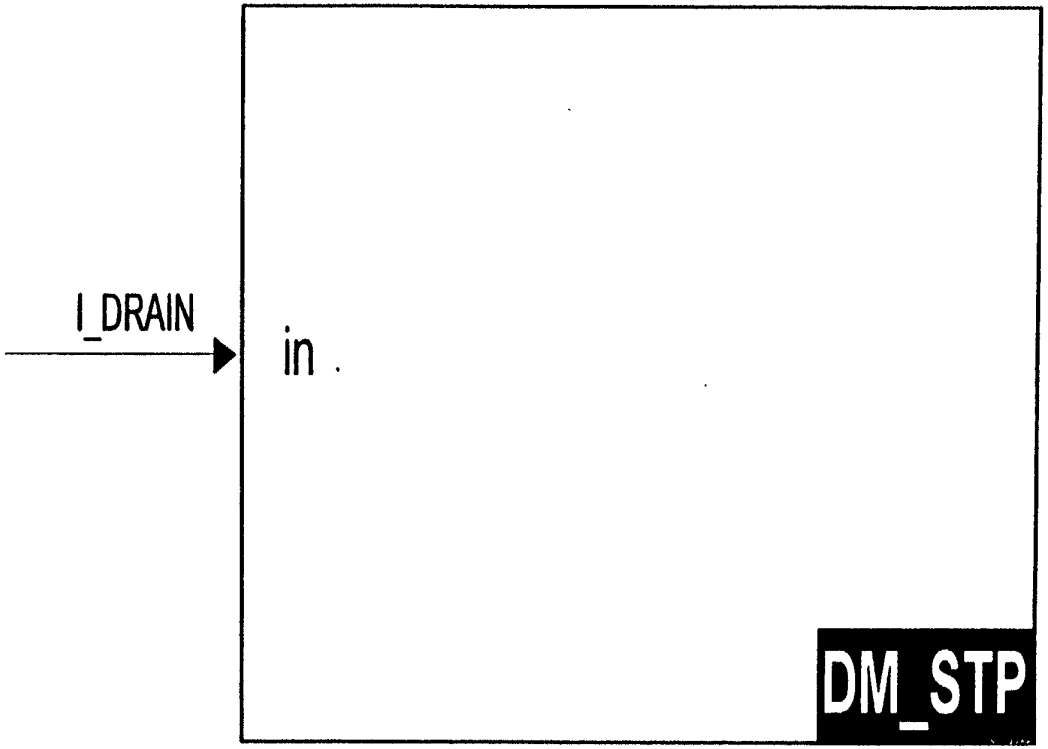


Fig. 66

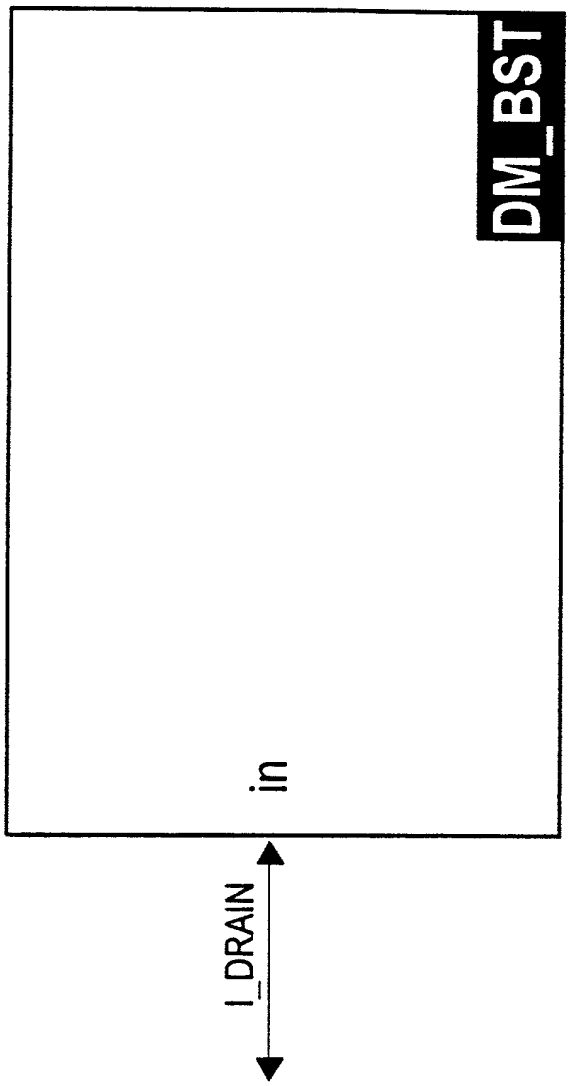


Fig. 67

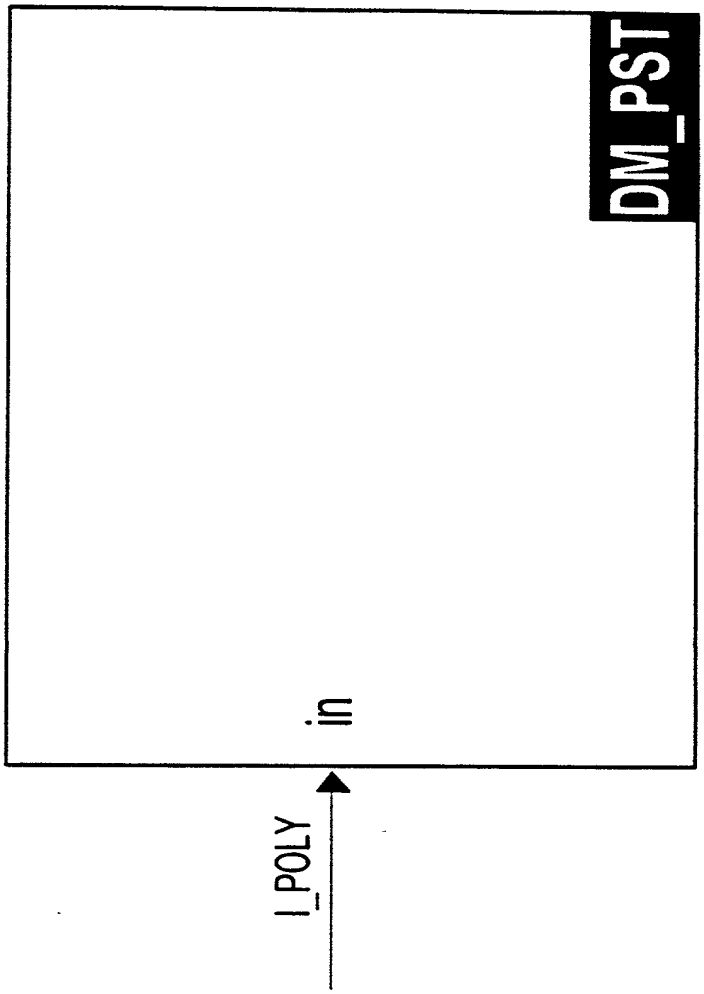


Fig. 68

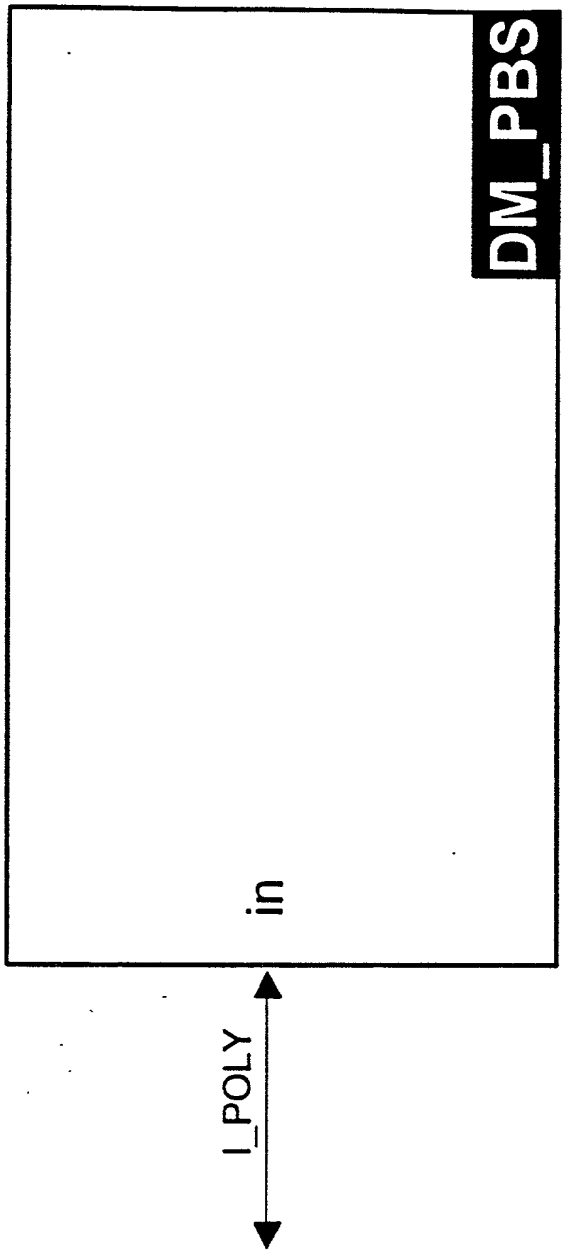


Fig. 69

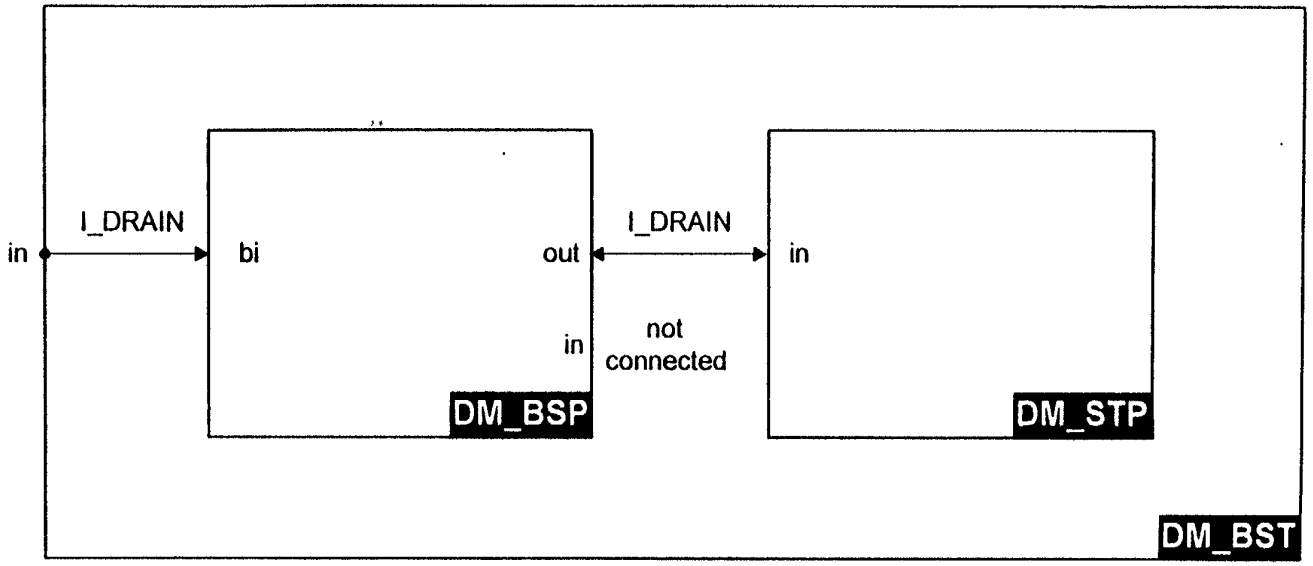

in
I_DRAIN
bi
out
in
DM_BSP
I_DRAIN
not
connected
in
DM_STP
DM_BST

Fig. 70

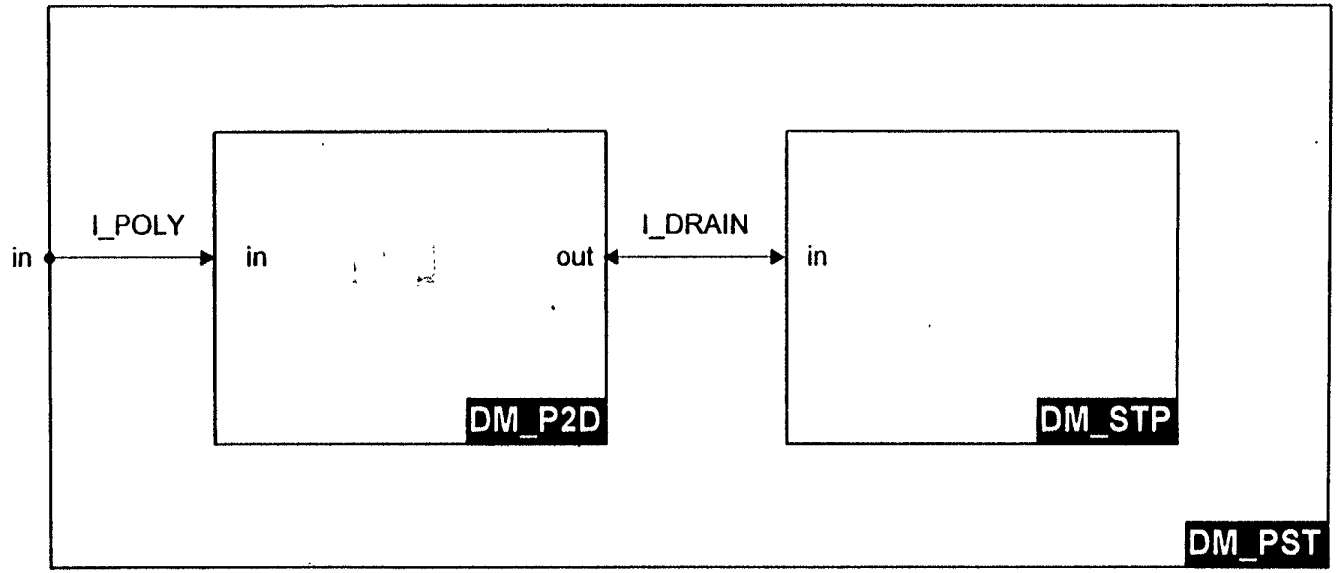


Fig. 71

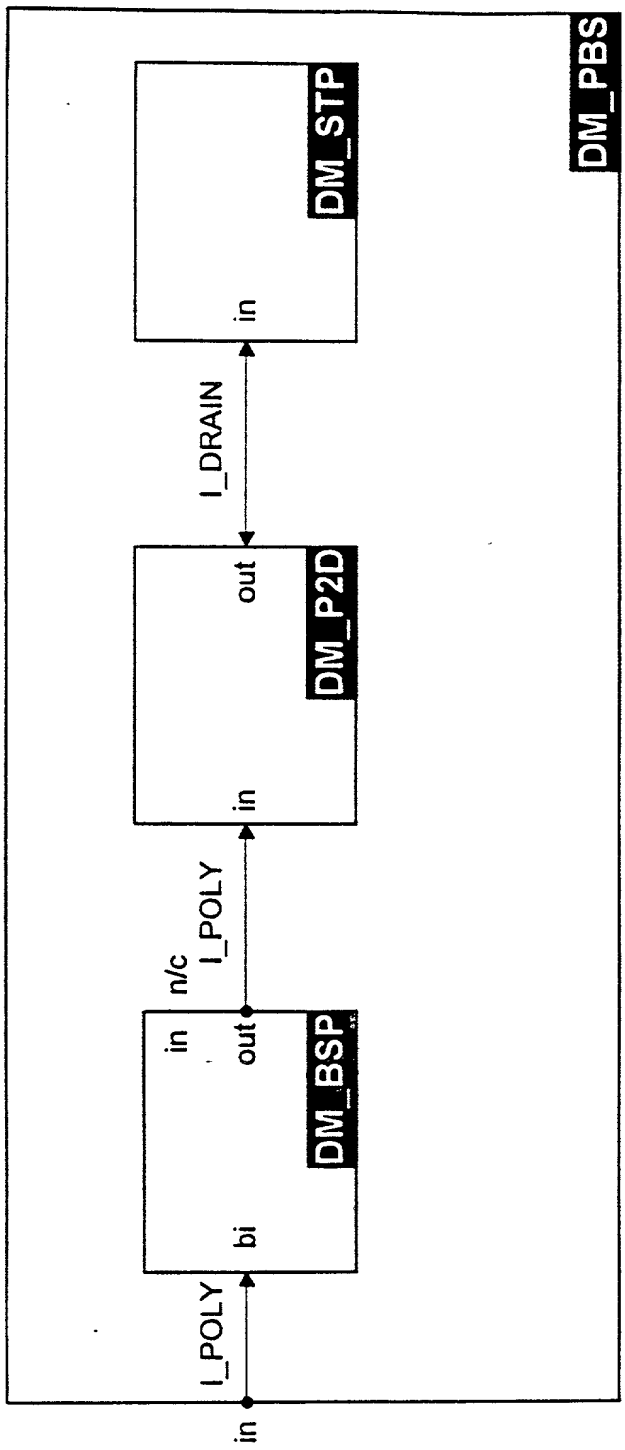

DM_PBS
DM_STP
in
I_DRAIN
DM_P2D
out
in
n/c
I_POLY
DM_BSP
in
out
bi
I_POLY
in

Fig. 72

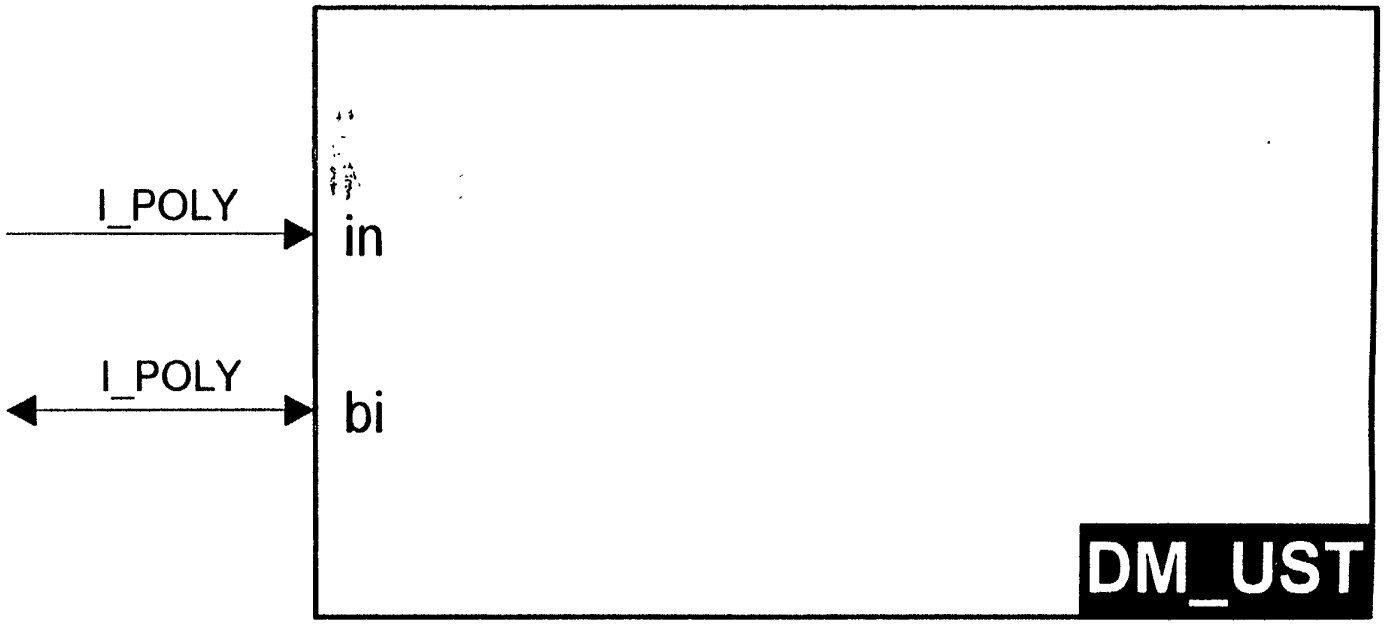


Fig. 73

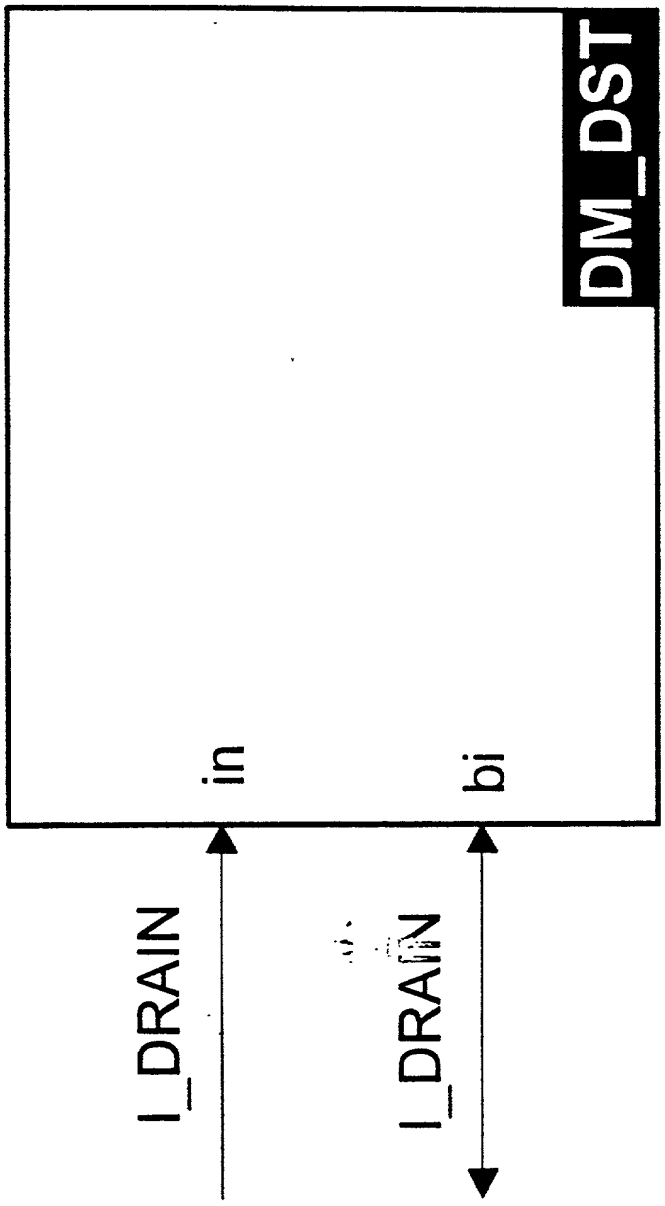


Fig. 74

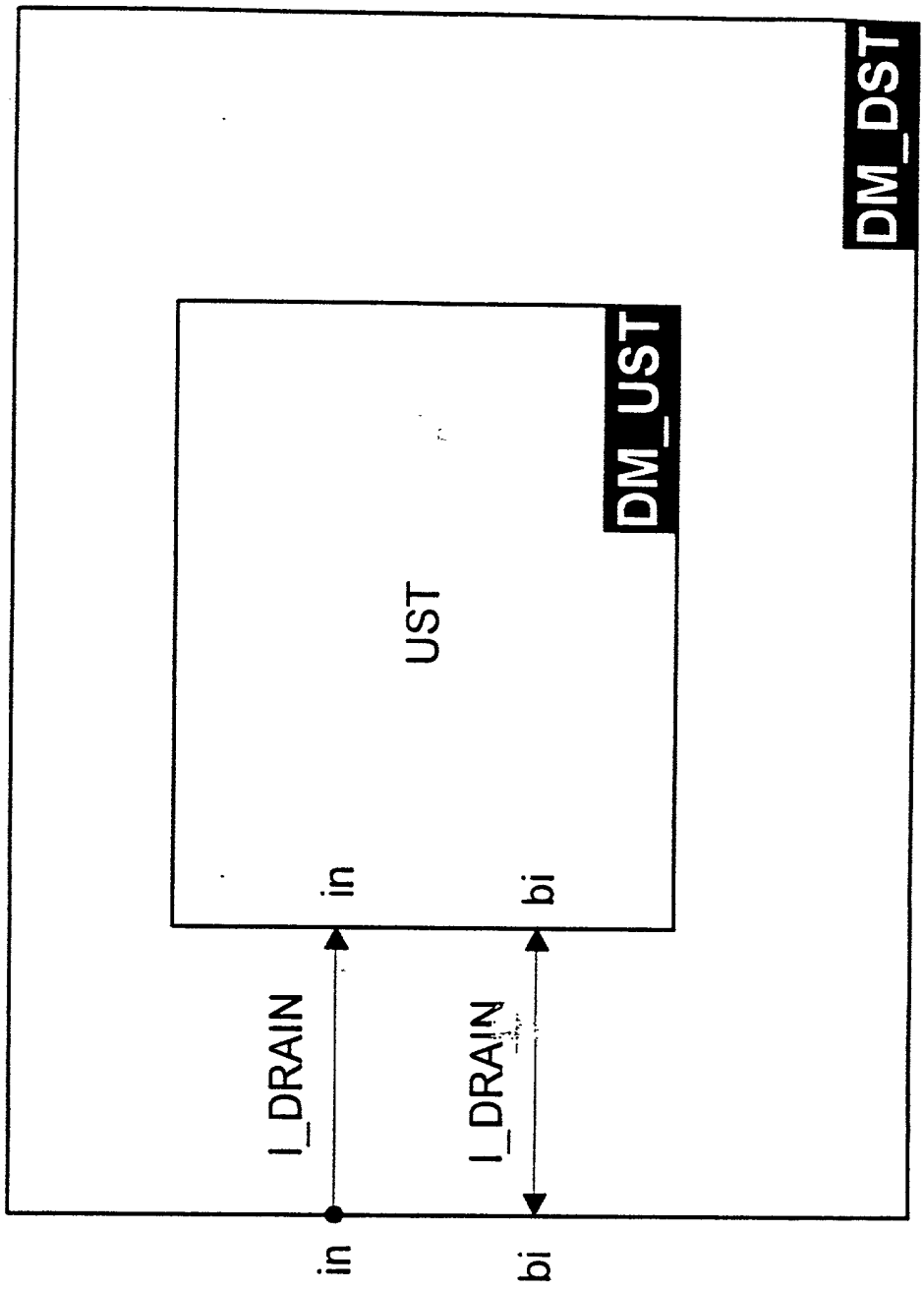


Fig. 75

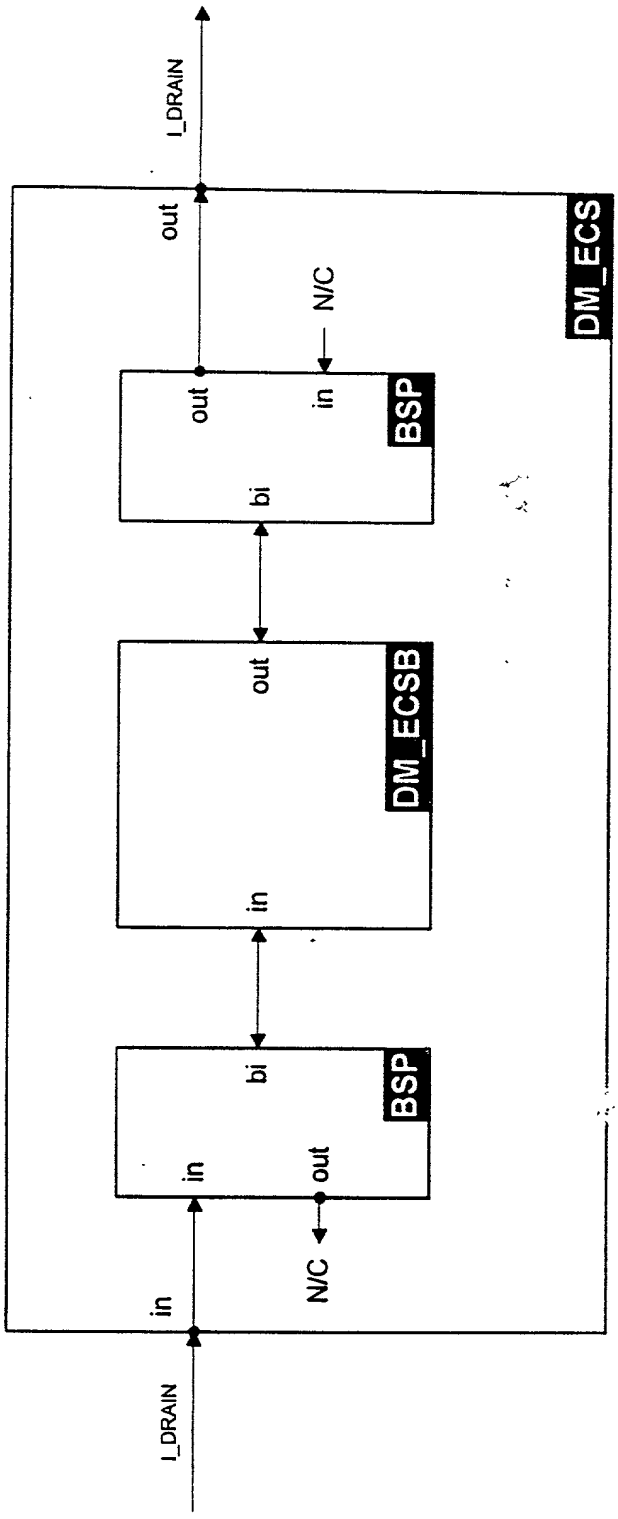

I_DRAIN
out
DM_ECS
N/C
out
in
BSP
bi
out
DM_ECSB
in
bi
BSP
in
out
N/C
in
I_DRAIN

Fig. 76

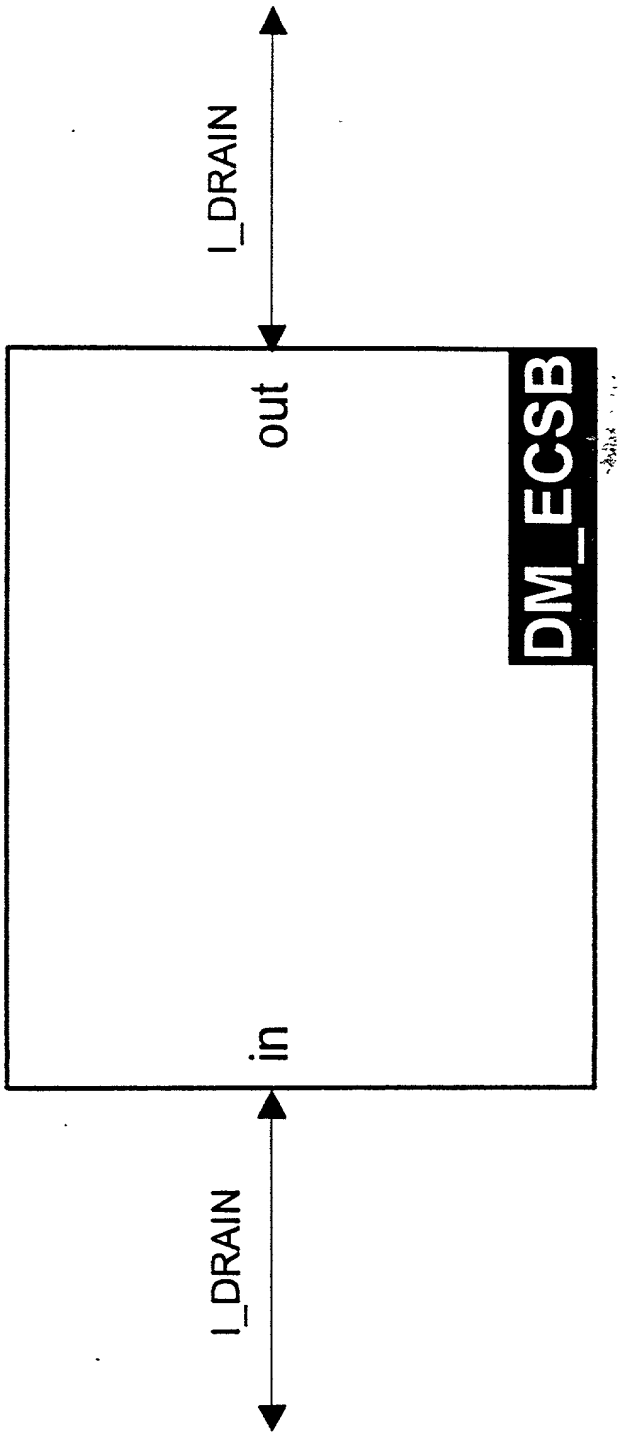


Fig. 77

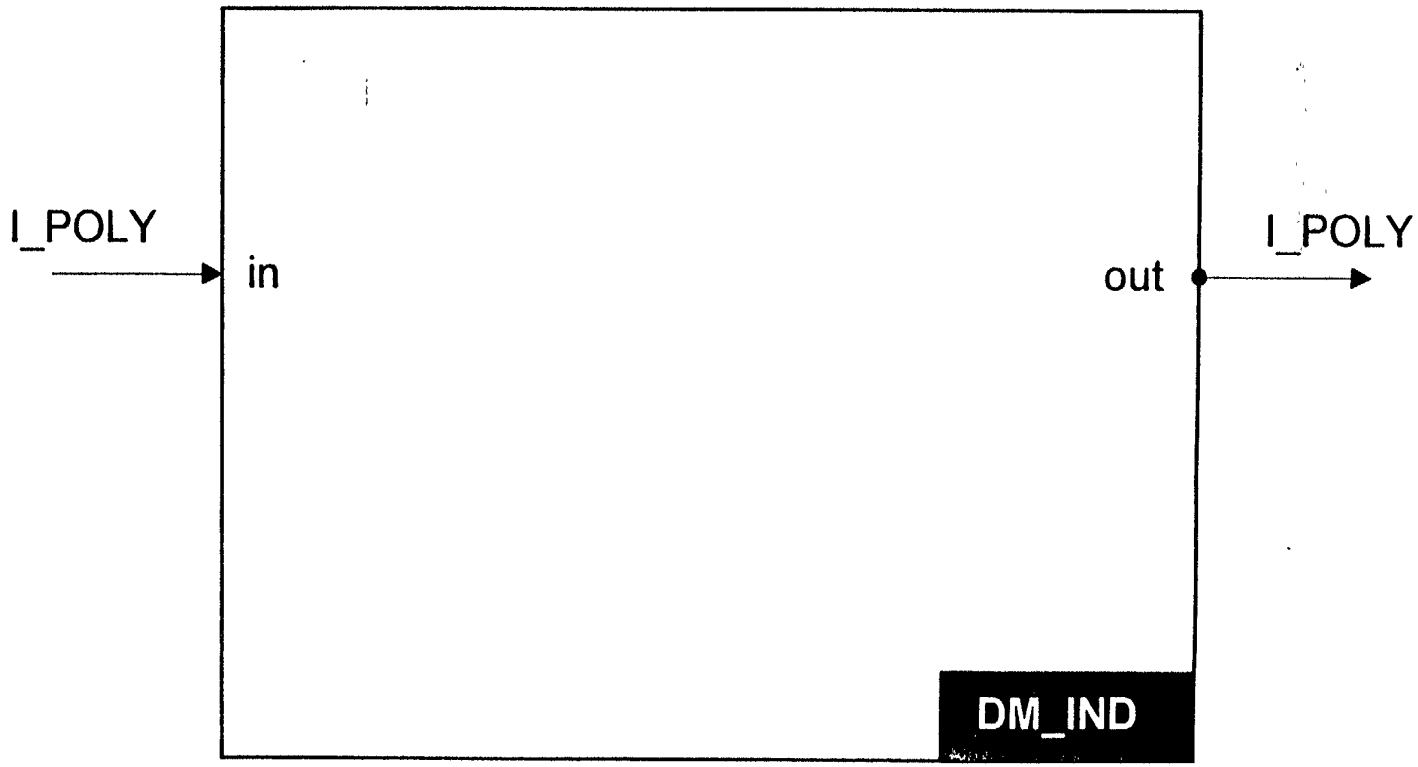


Fig. 78

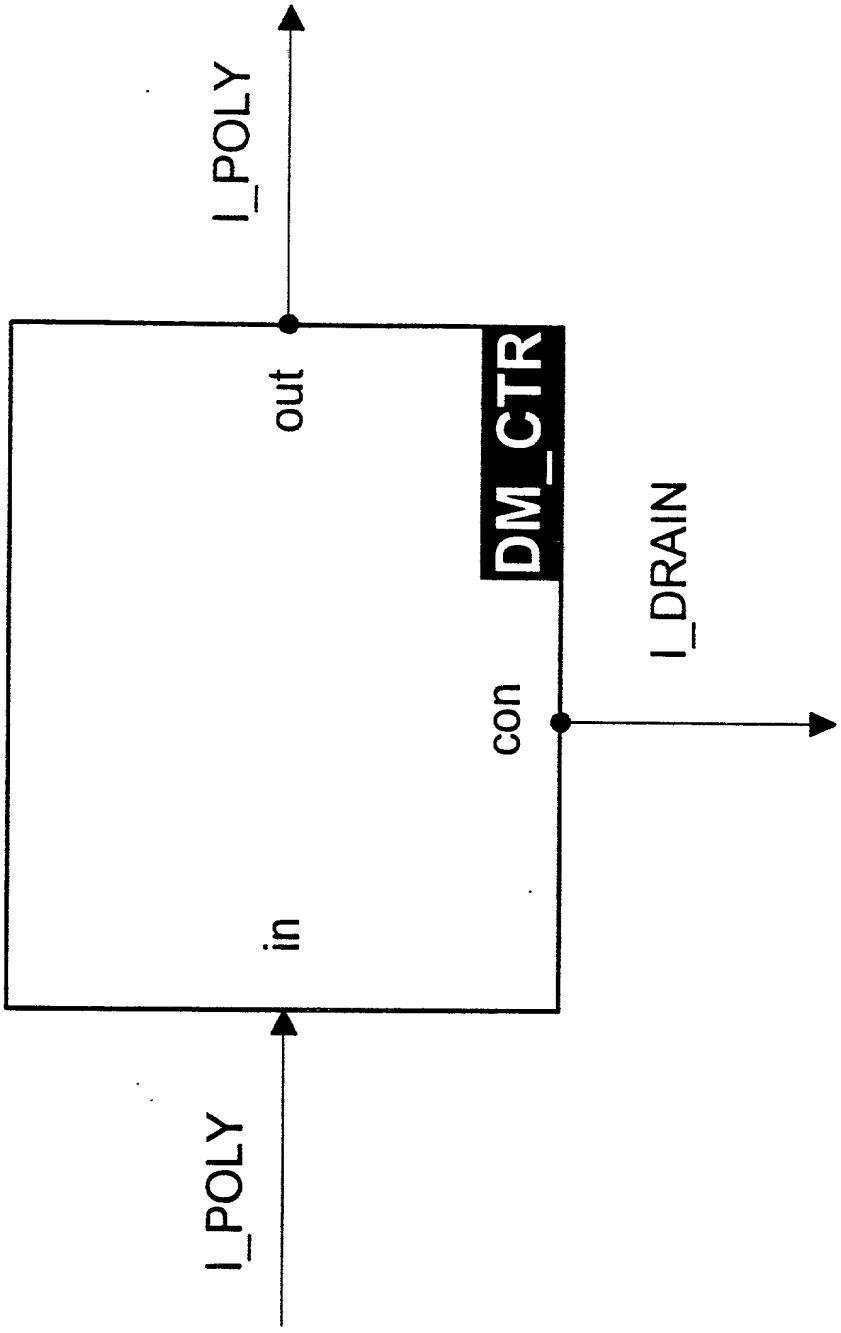


Fig. 79

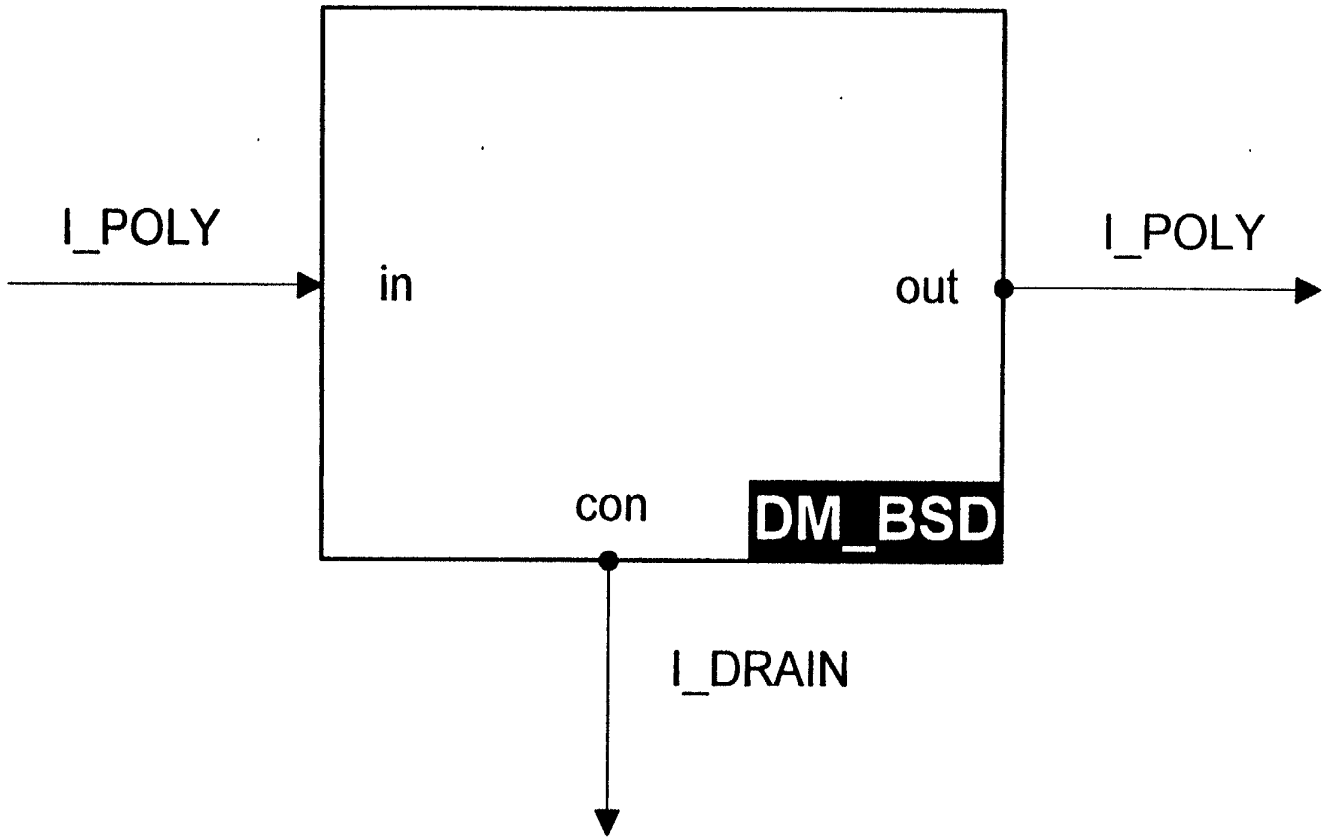


Fig. 80

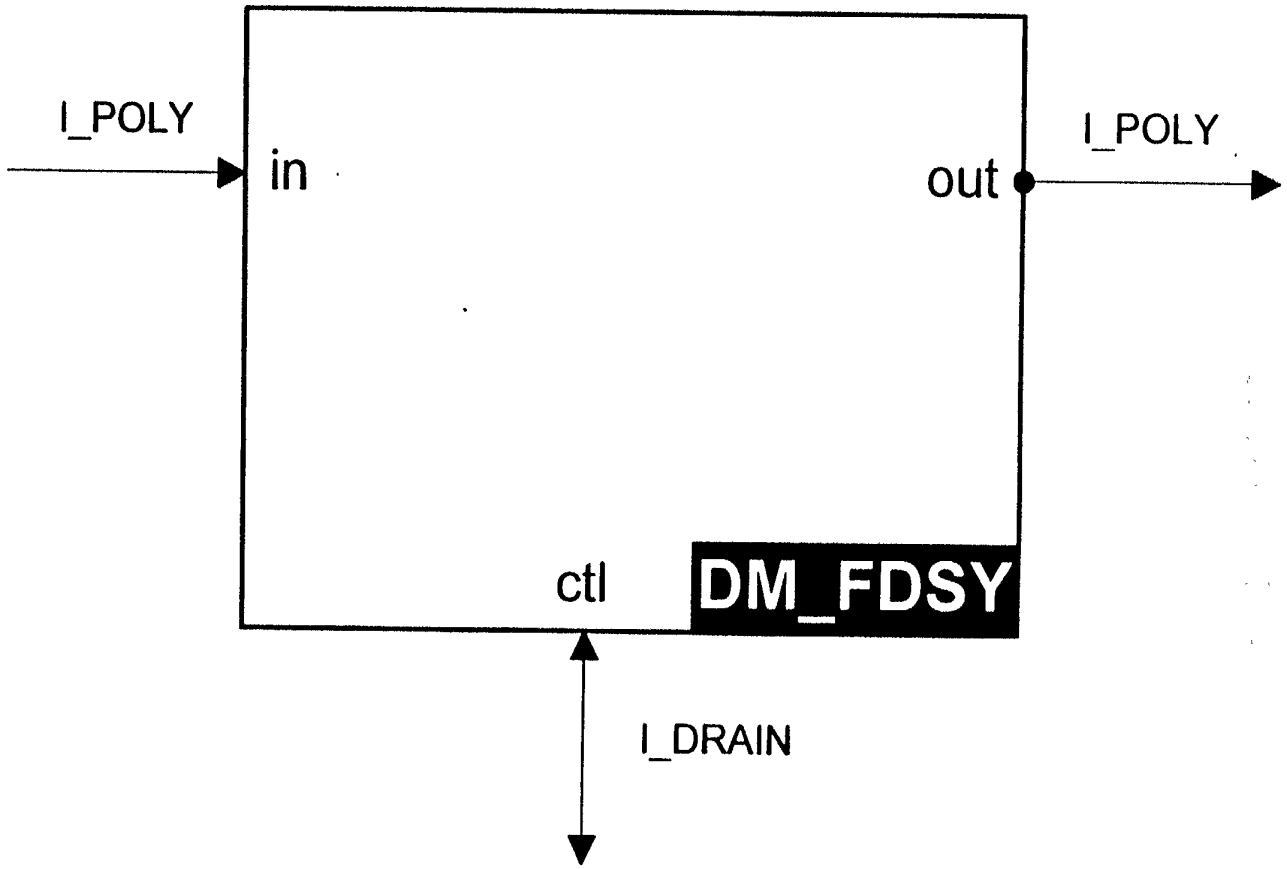


Fig. 81

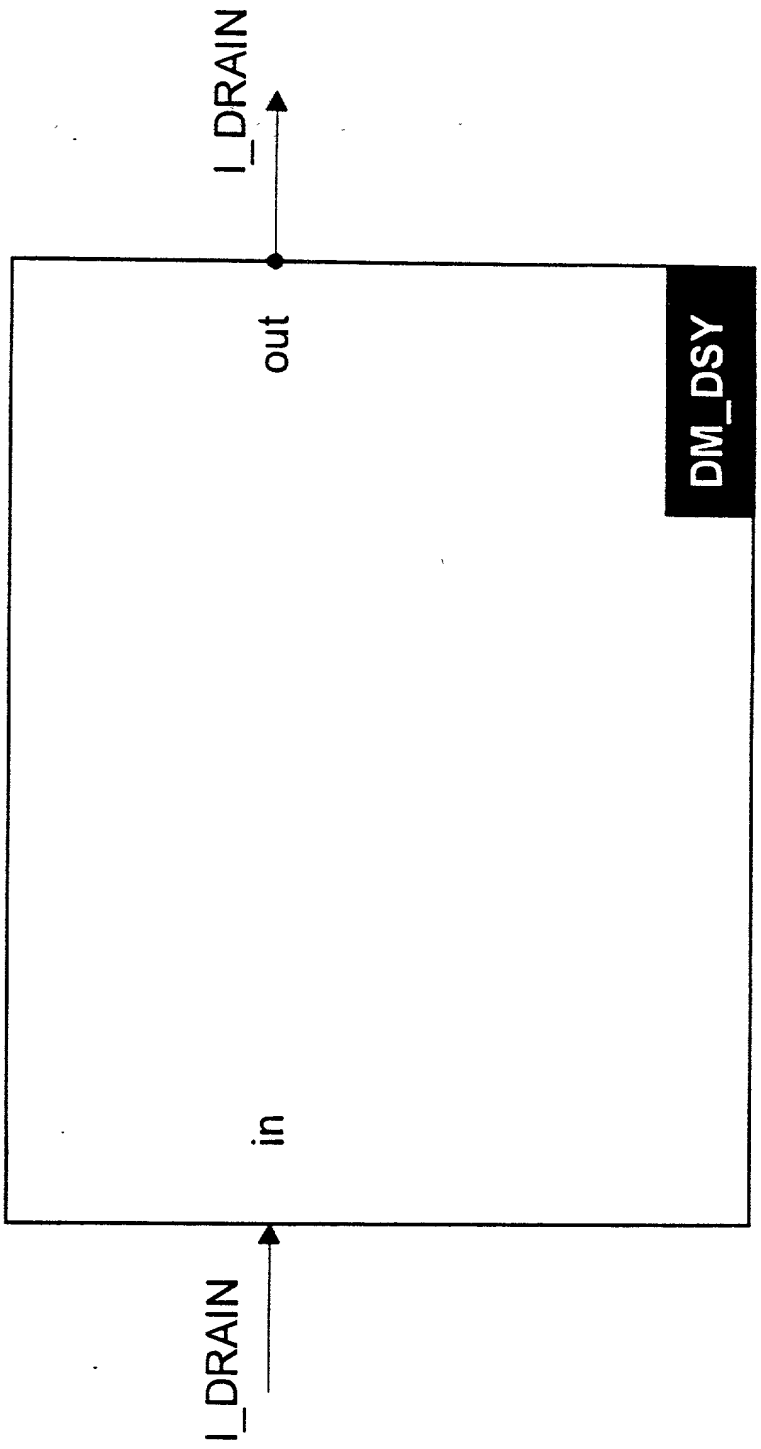


Fig. 82

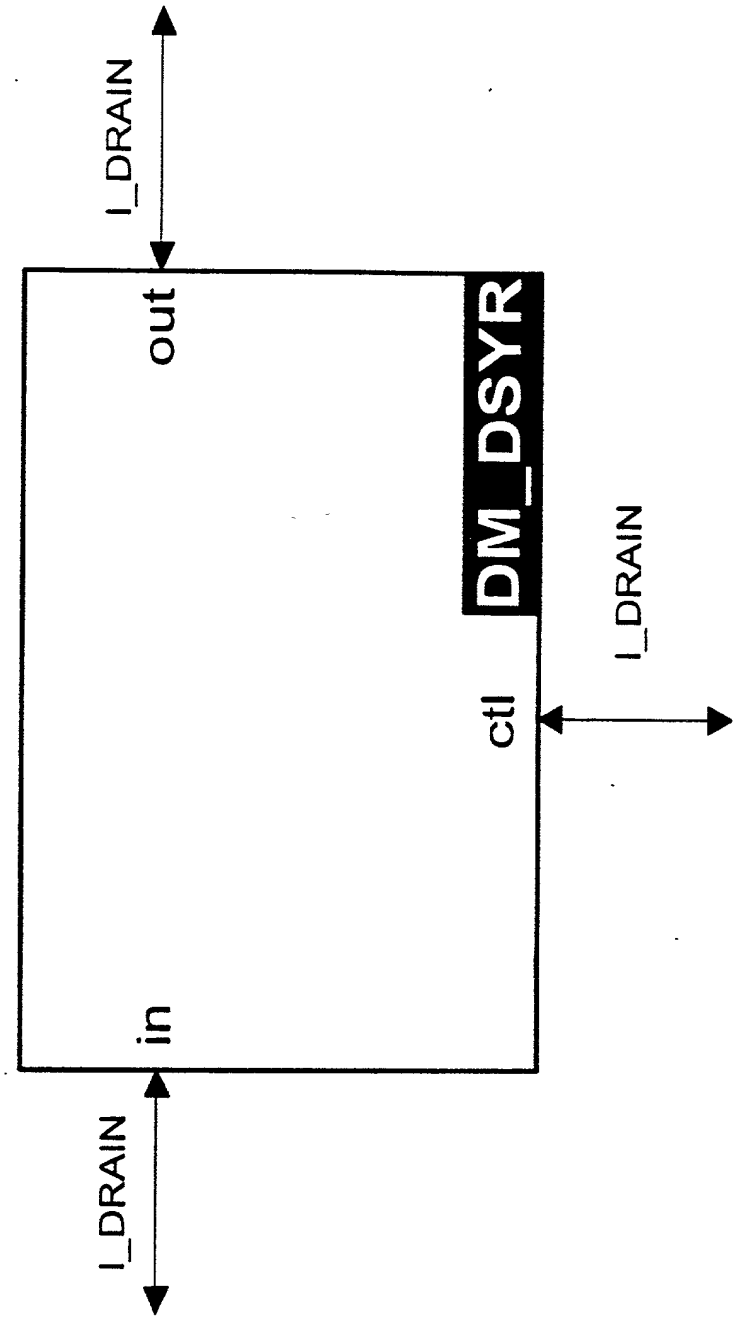


Fig. 83

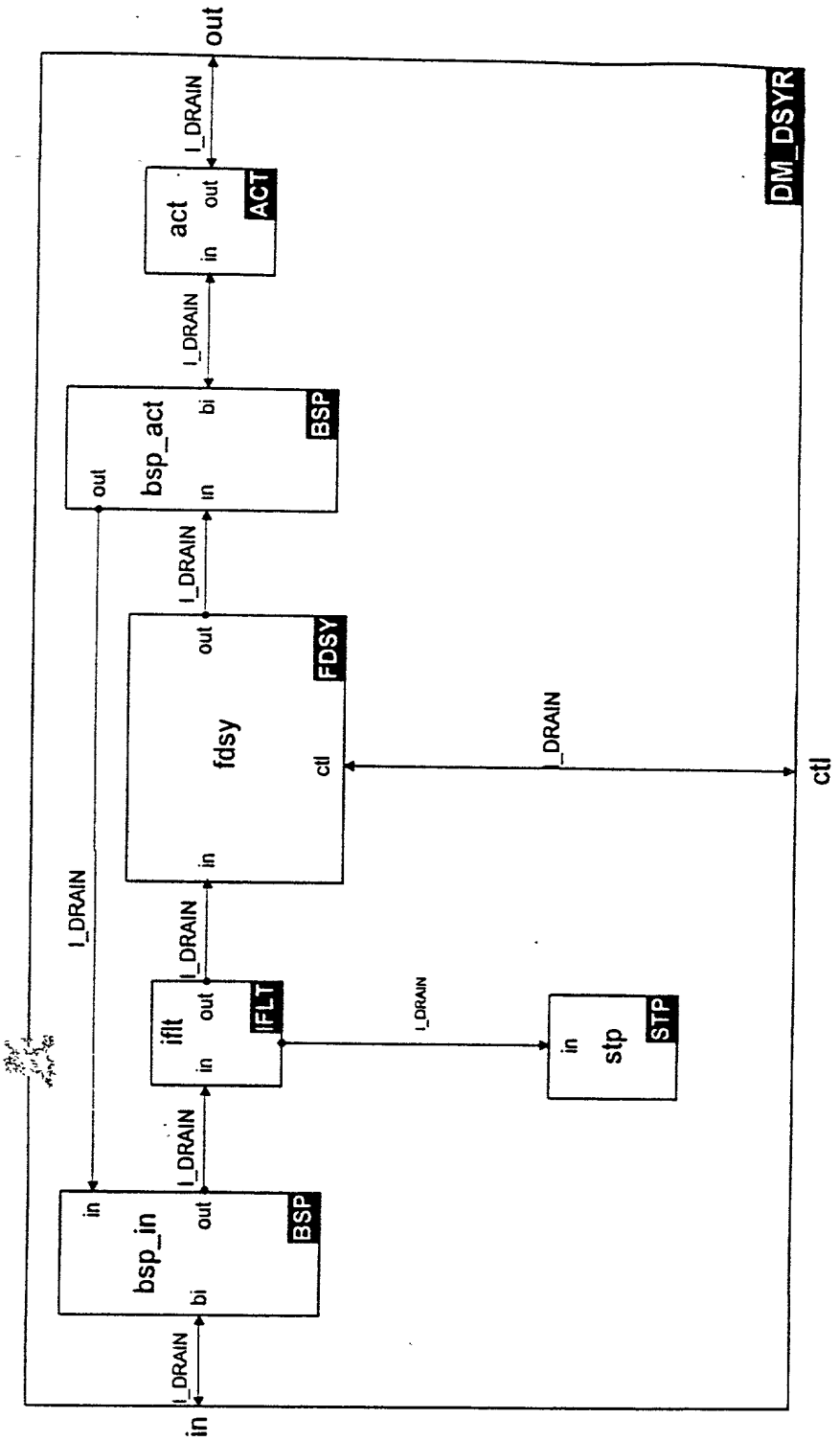

DM_DSYR
in
out
ctl
I_DRAIN
bsp_in
BSP
ifilt
IFLT
fdsy
FDSY
bsp_act
BSP
act
ACT
stp
STP
in
out
bi

Fig. 84

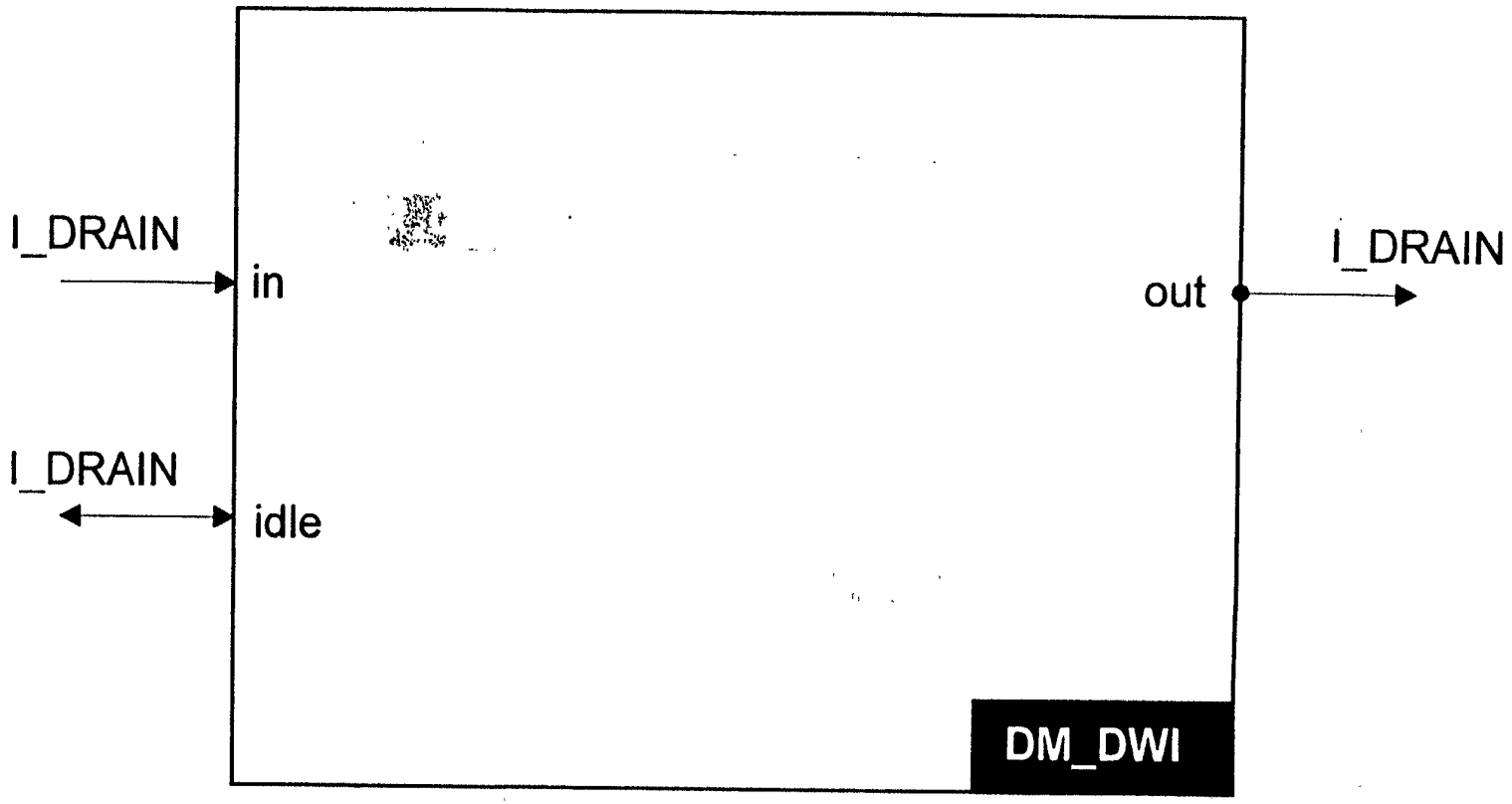


Fig. 85

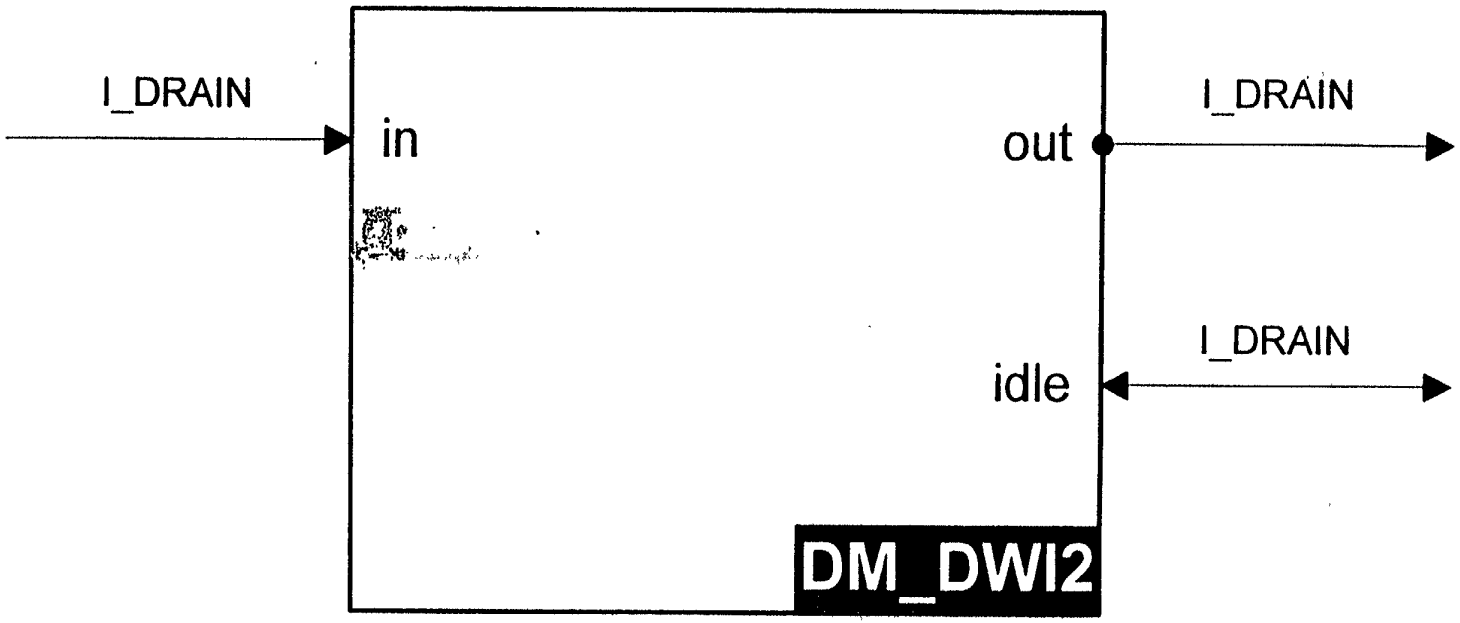


Fig. 86

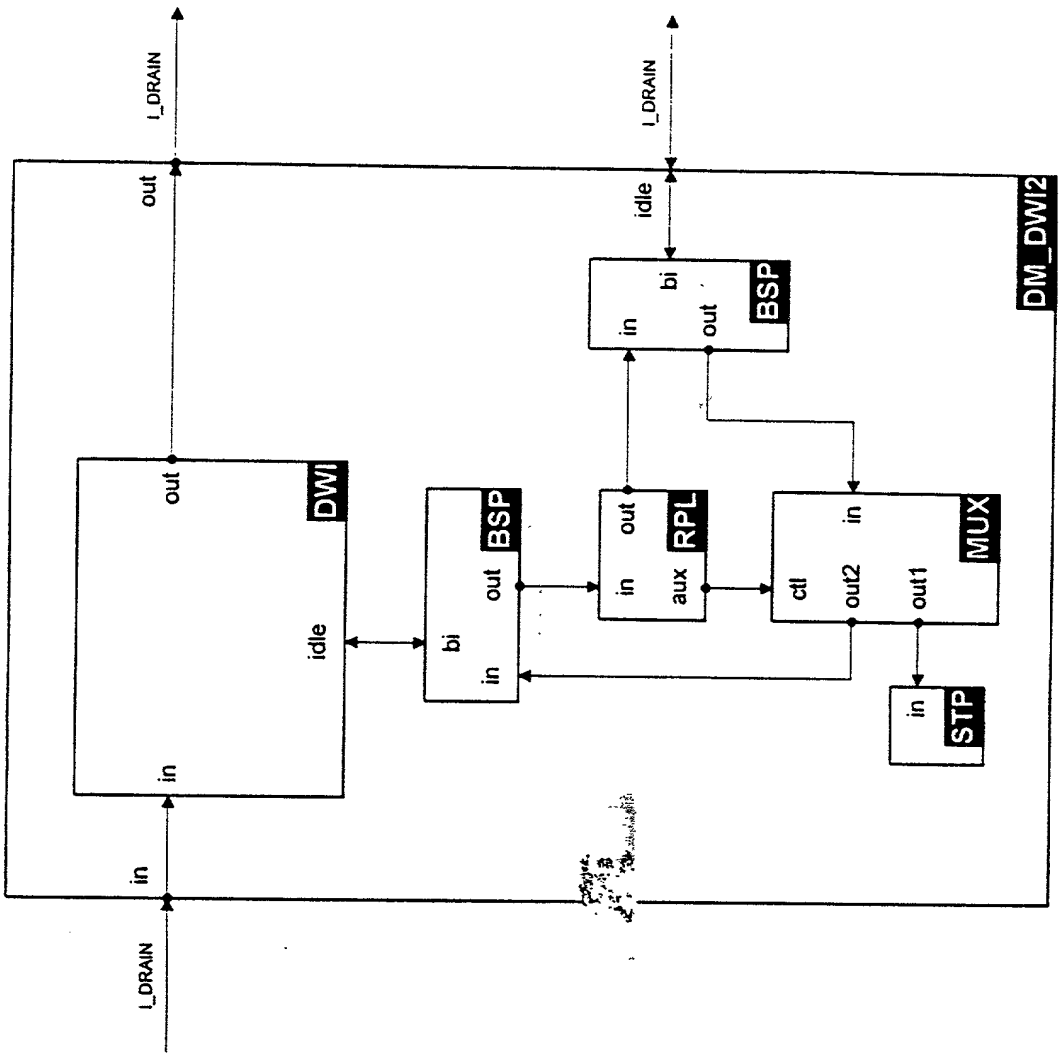

I_DRAIN
I_DRAIN
out
idle
bi
in
out
BSP
DM_DWI2
out
DWI
idle
in
bi
out
BSP
in
out
aux
RPL
ctl
out2
in
out1
MUX
in
STP
in
I_DRAIN

Fig. 87

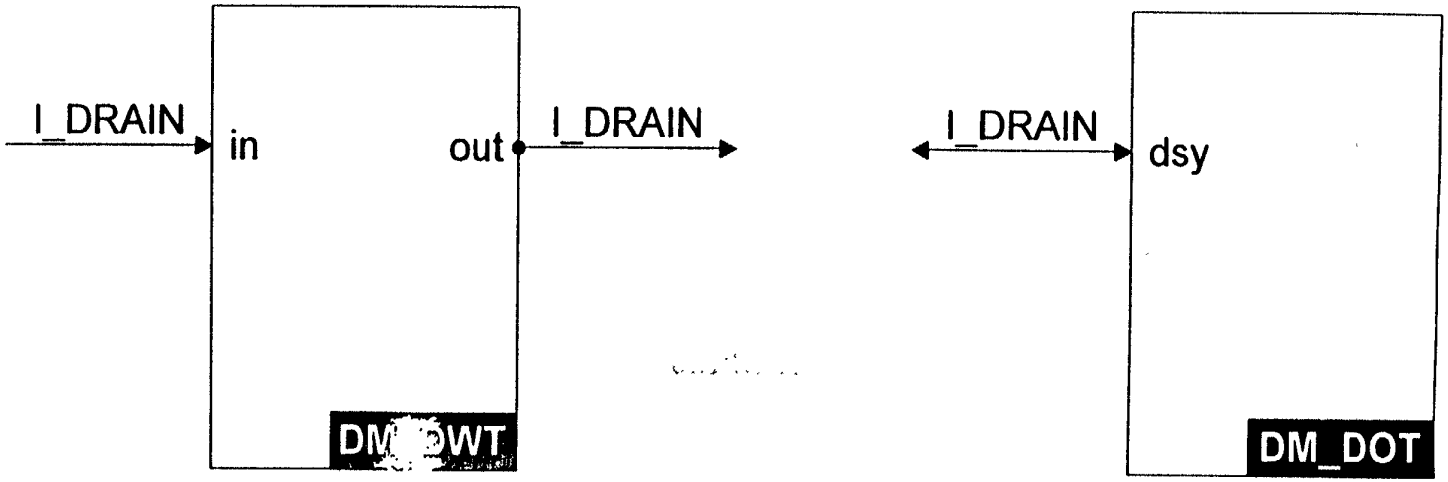


Fig. 88

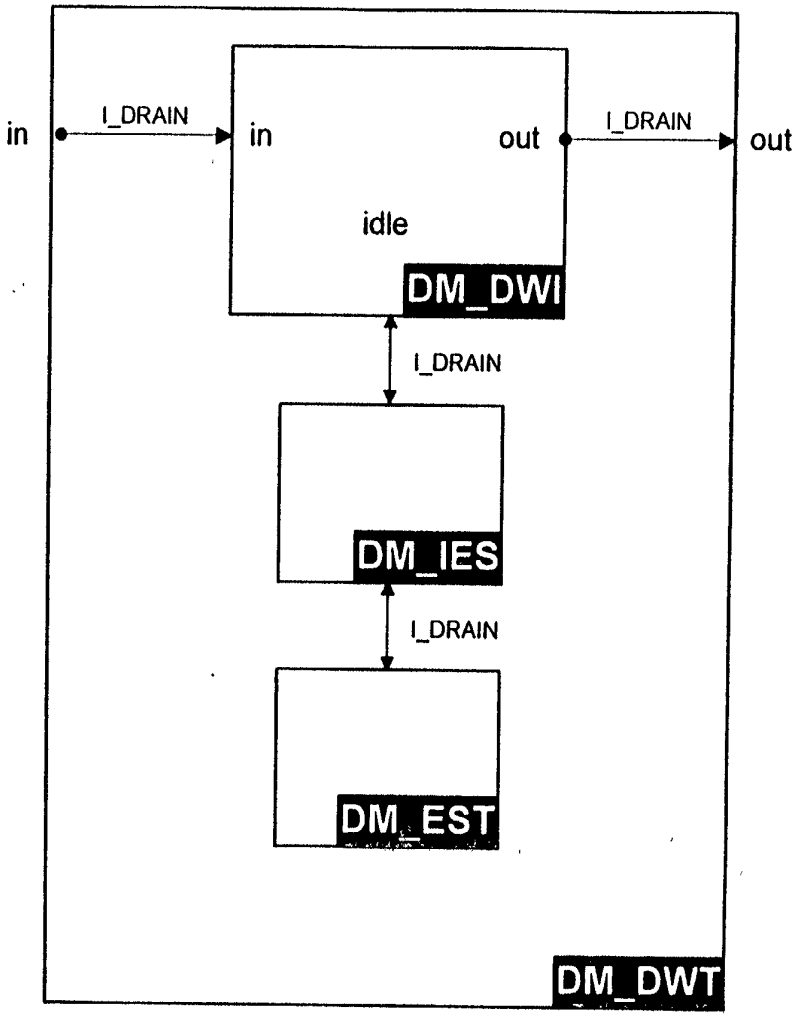

in
I_DRAIN
in
out
I_DRAIN
out
idle
DM_DWI
I_DRAIN
DM_IES
I_DRAIN
DM_EST
DM_DWT

Fig. 89

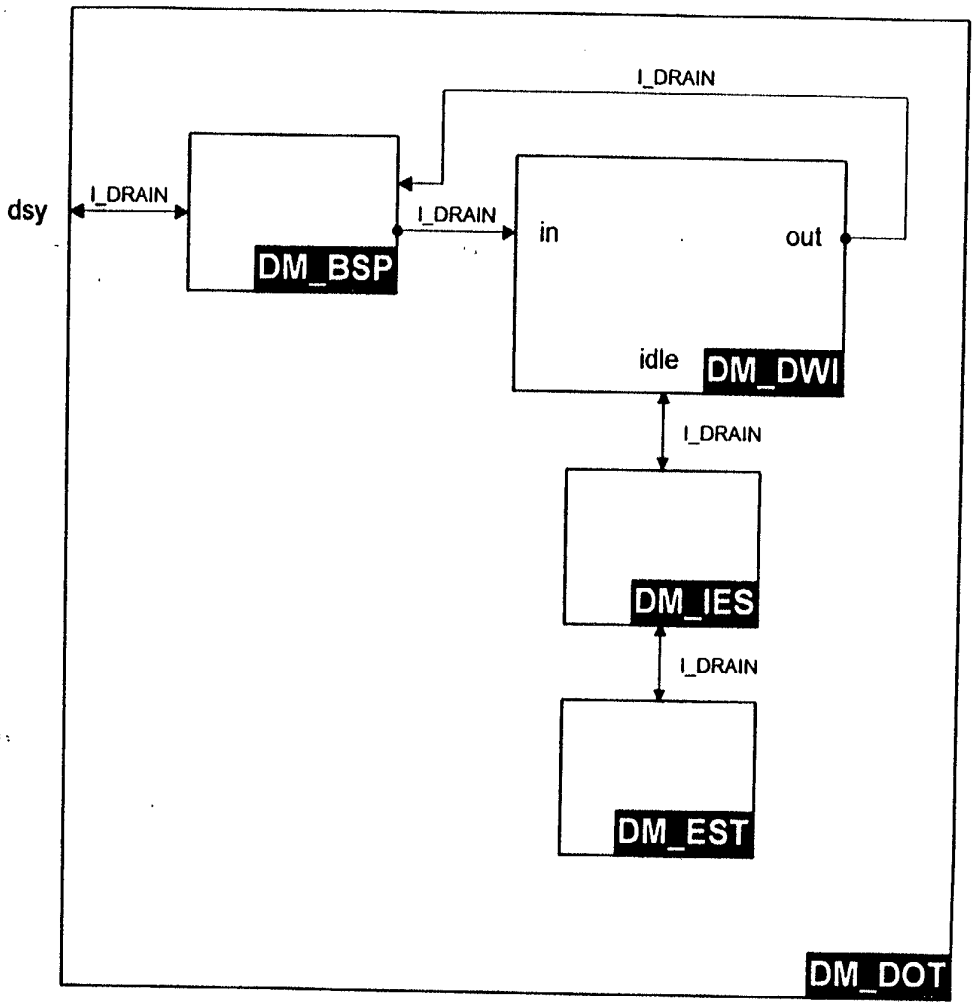

I_DRAIN
dsy
I_DRAIN
DM_BSP
I_DRAIN
in
out
idle
DM_DWI
I_DRAIN
DM_IES
I_DRAIN
DM_EST
DM_DOT

Fig. 90

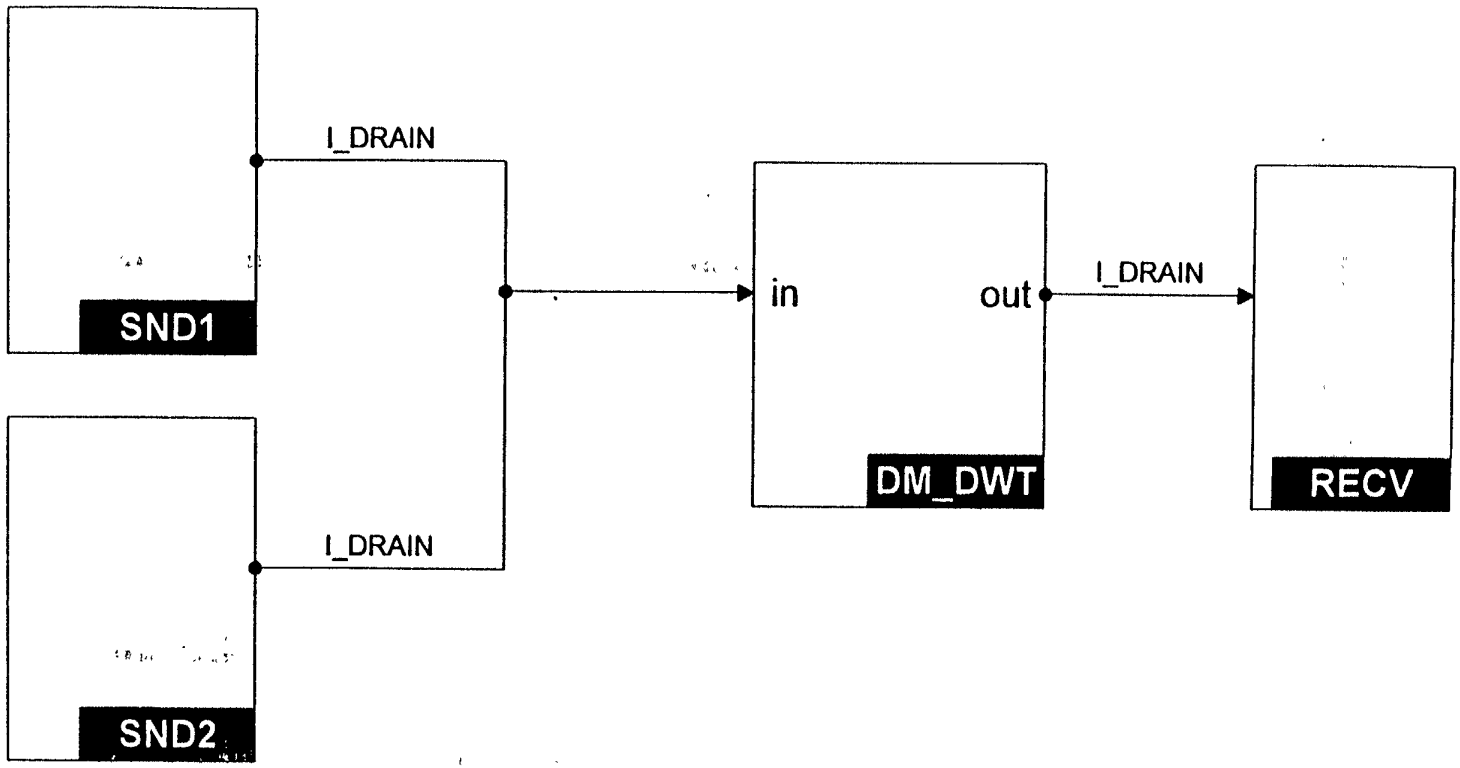


Fig. 91

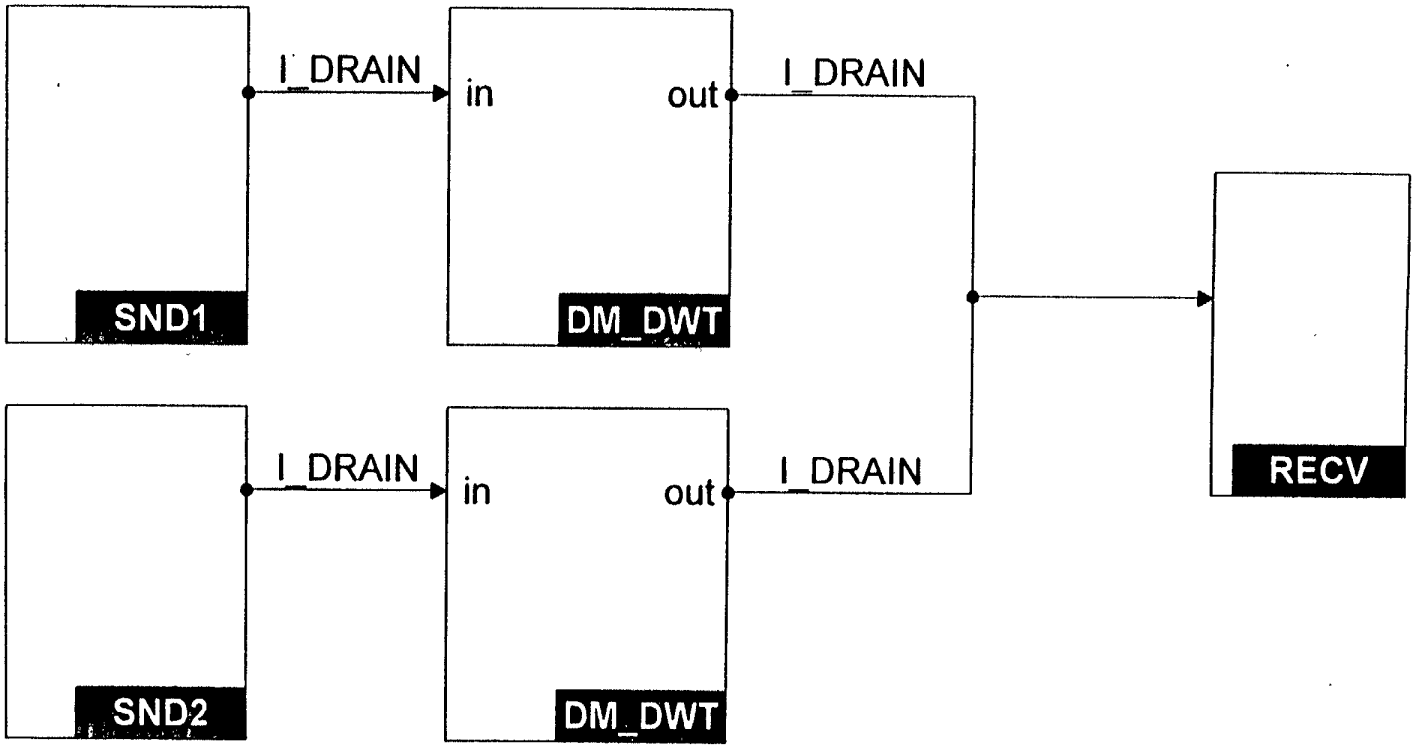

I_DRAIN
in
out
I_DRAIN
SND1
DM_DWT
I_DRAIN
in
out
I_DRAIN
SND2
DM_DWT
RECV

Fig. 92

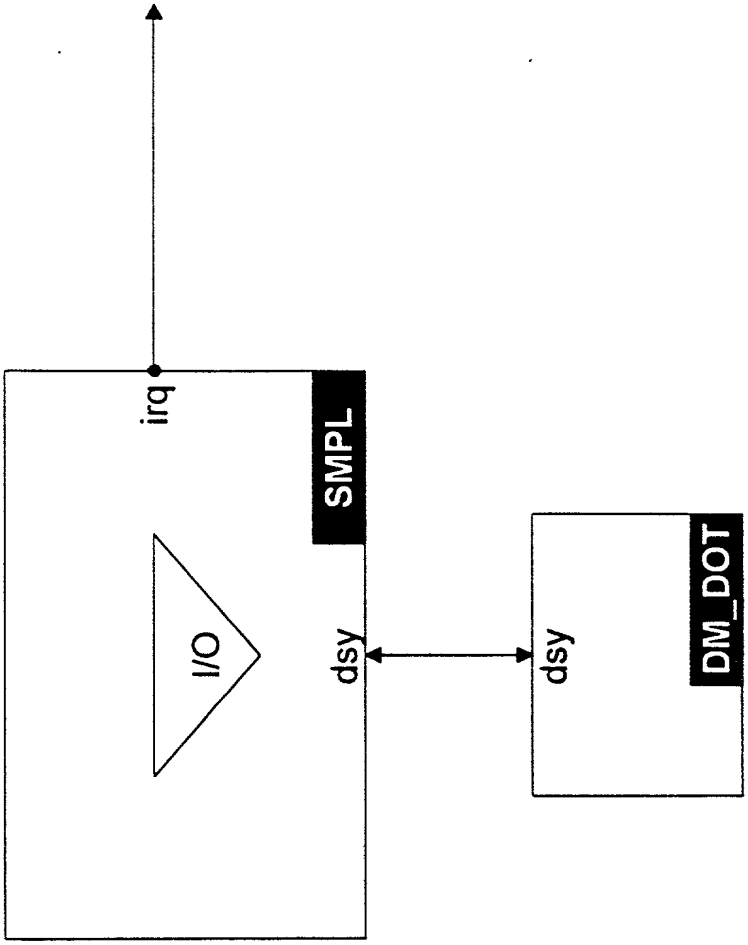


Fig. 93

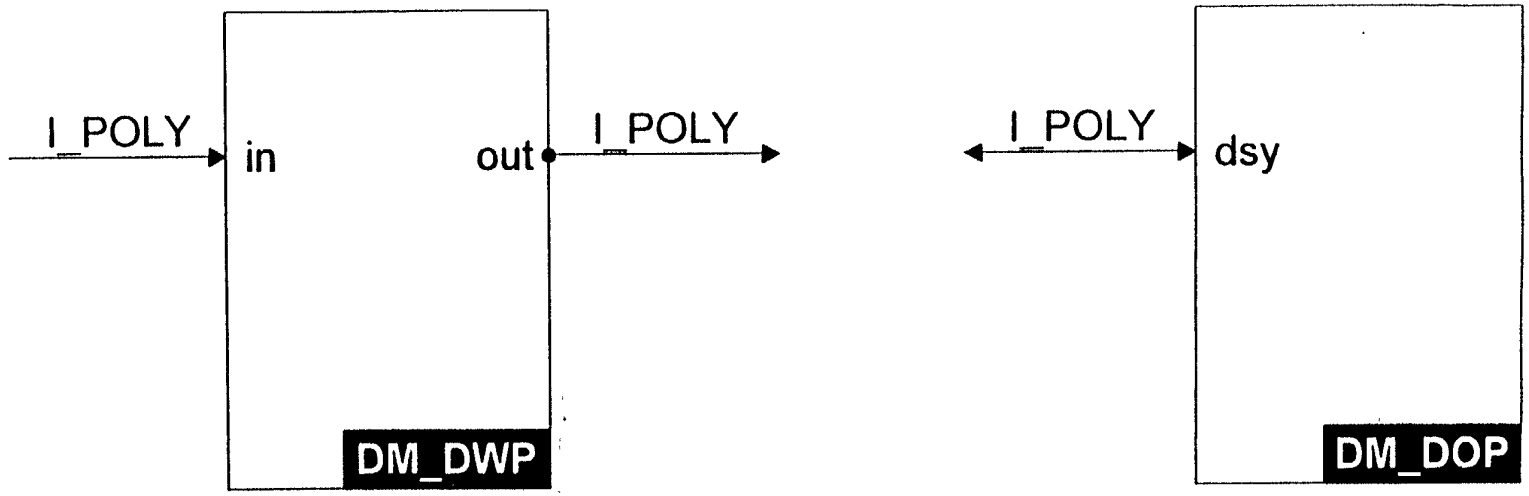


Fig. 94

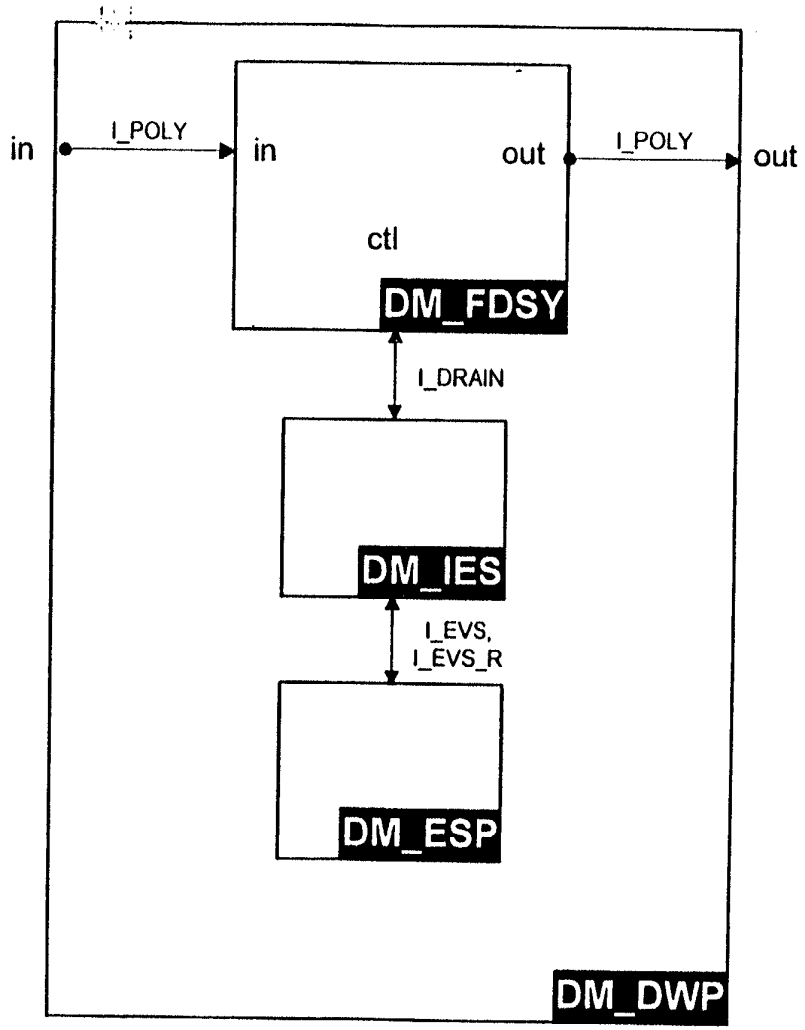

in
I_POLY
in
out
I_POLY
out
ctl
DM_FDSY
I_DRAIN
DM_IES
I_EVS,
I_EVS_R
DM_ESP
DM_DWP

Fig. 95

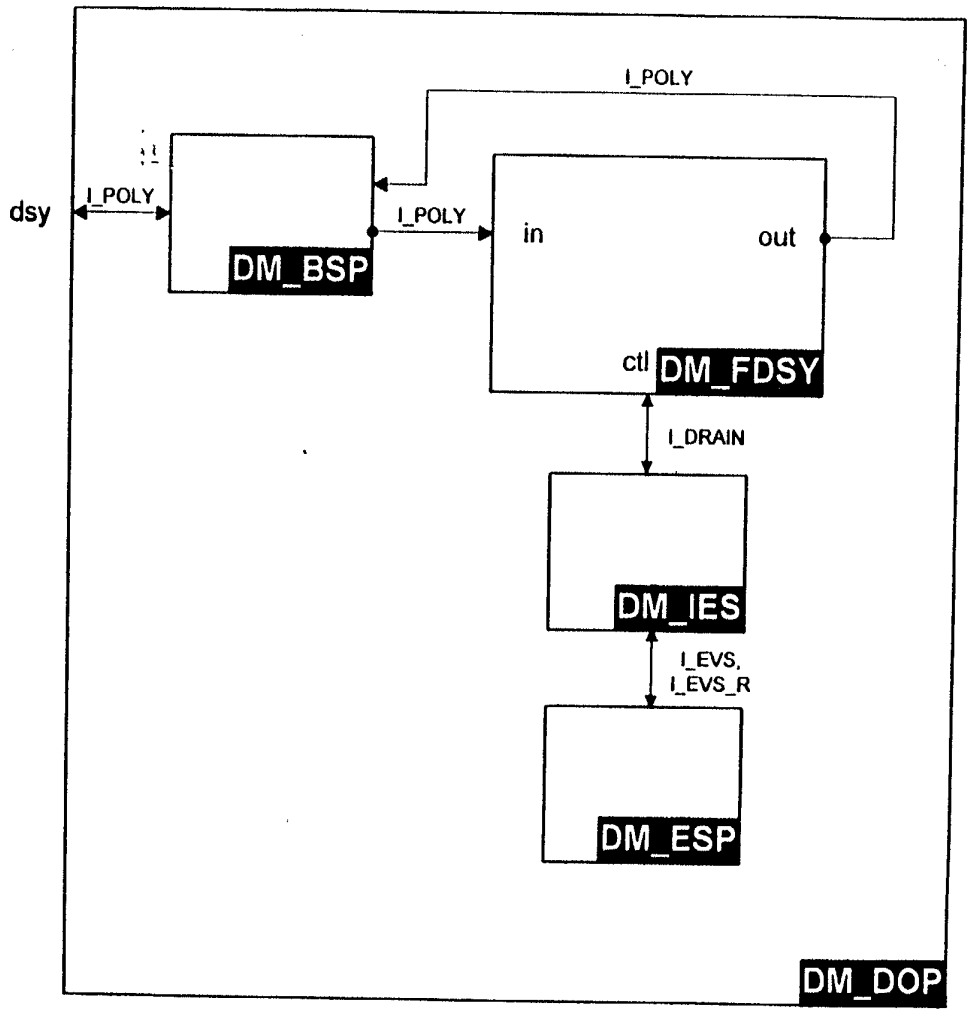

I_POLY
dsy
I_POLY
DM_BSP
I_POLY
in
out
ctl
DM_FDSY
I_DRAIN
DM_IES
I_EVS,
I_EVS_R
DM_ESP
DM_DOP

Fig. 96

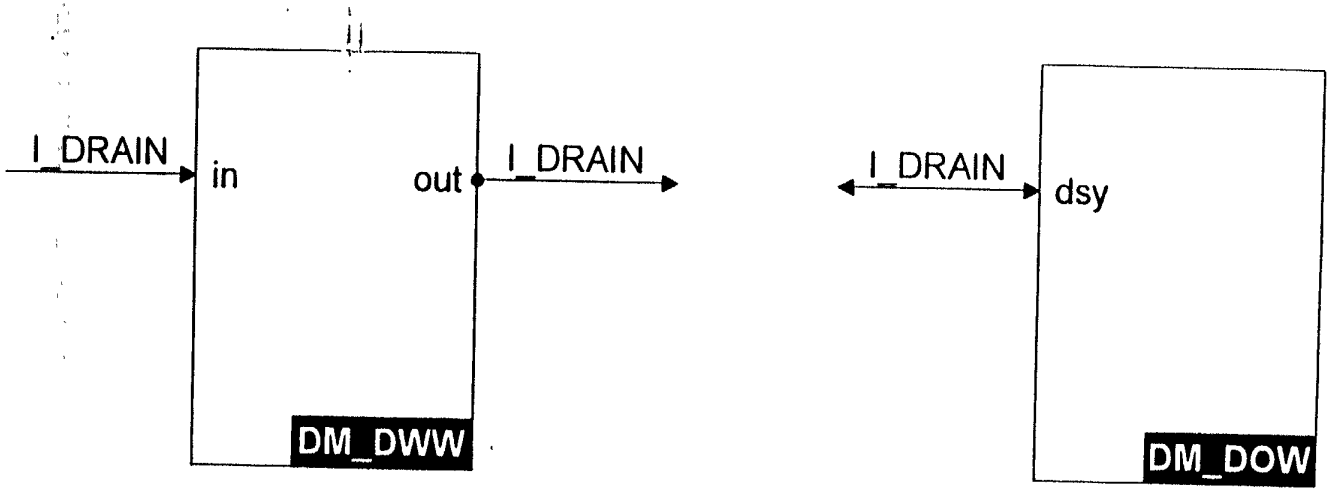


Fig. 97

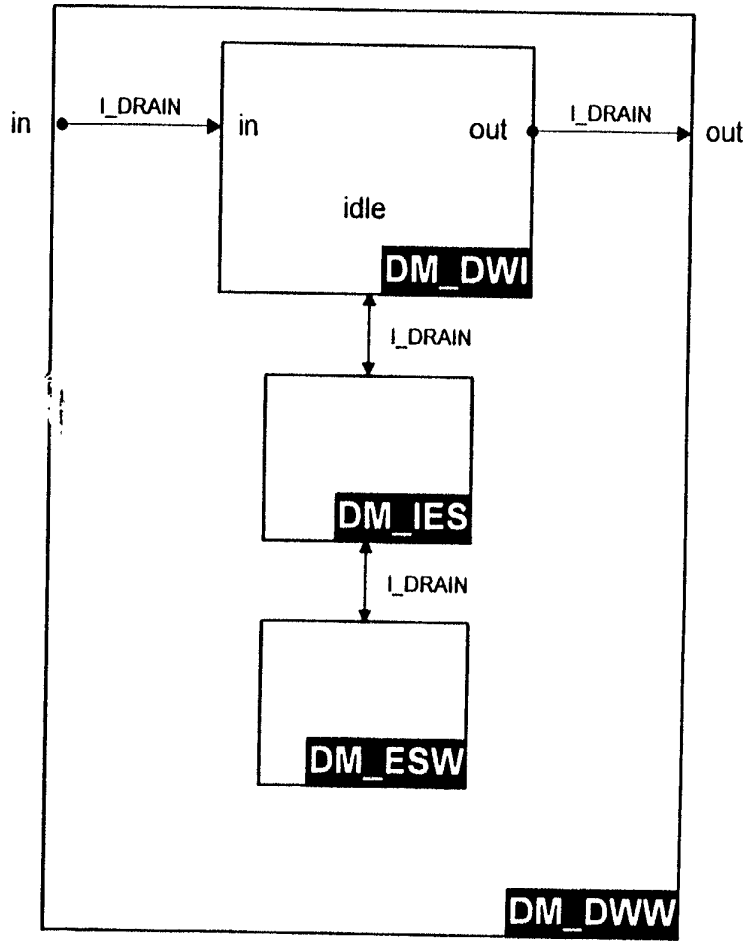

in
I_DRAIN
in
out
I_DRAIN
out
idle
DM_DWI
I_DRAIN
DM_IES
I_DRAIN
DM_ESW
DM_DWW

Fig. 98

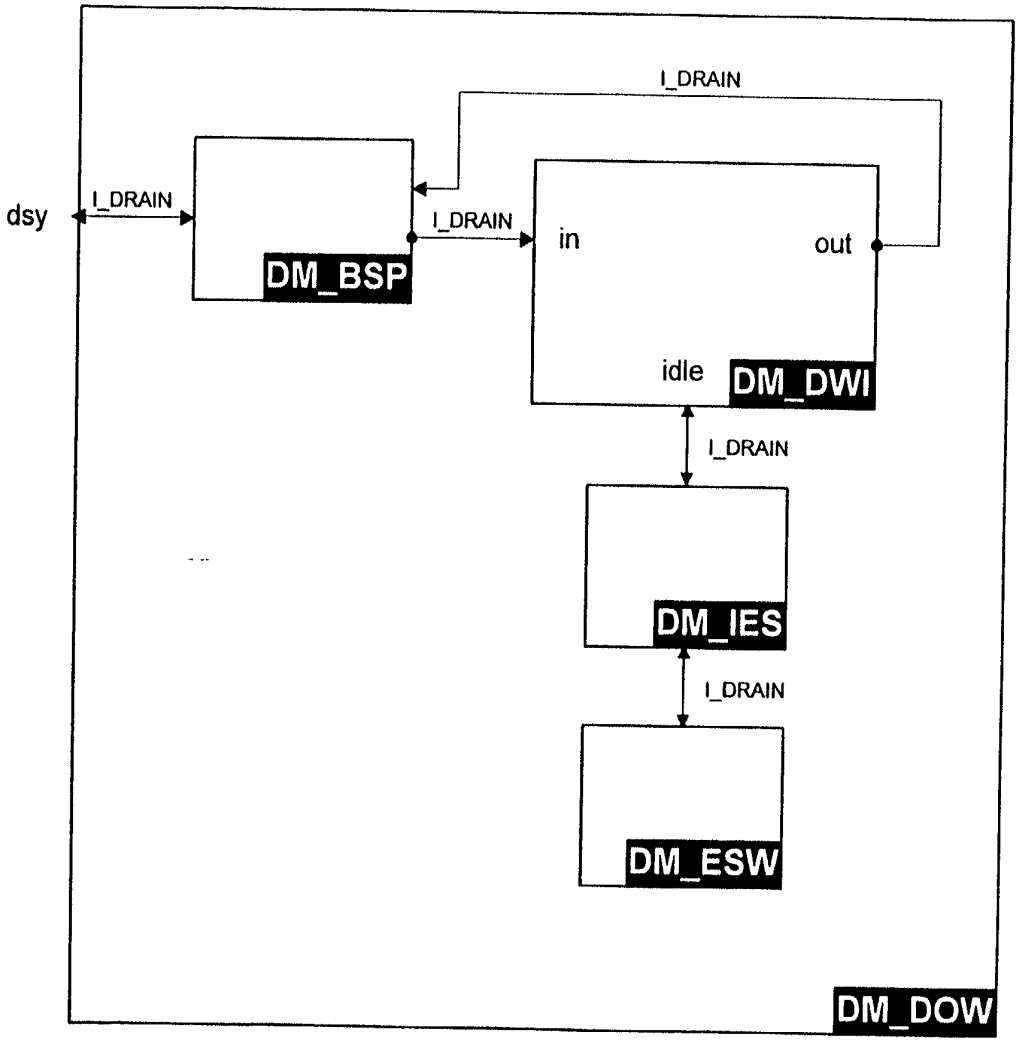

I_DRAIN
dsy
I_DRAIN
I_DRAIN
DM_BSP
in
out
idle
DM_DWI
I_DRAIN
DM_IES
I_DRAIN
DM_ESW
DM_DOW

Fig. 99

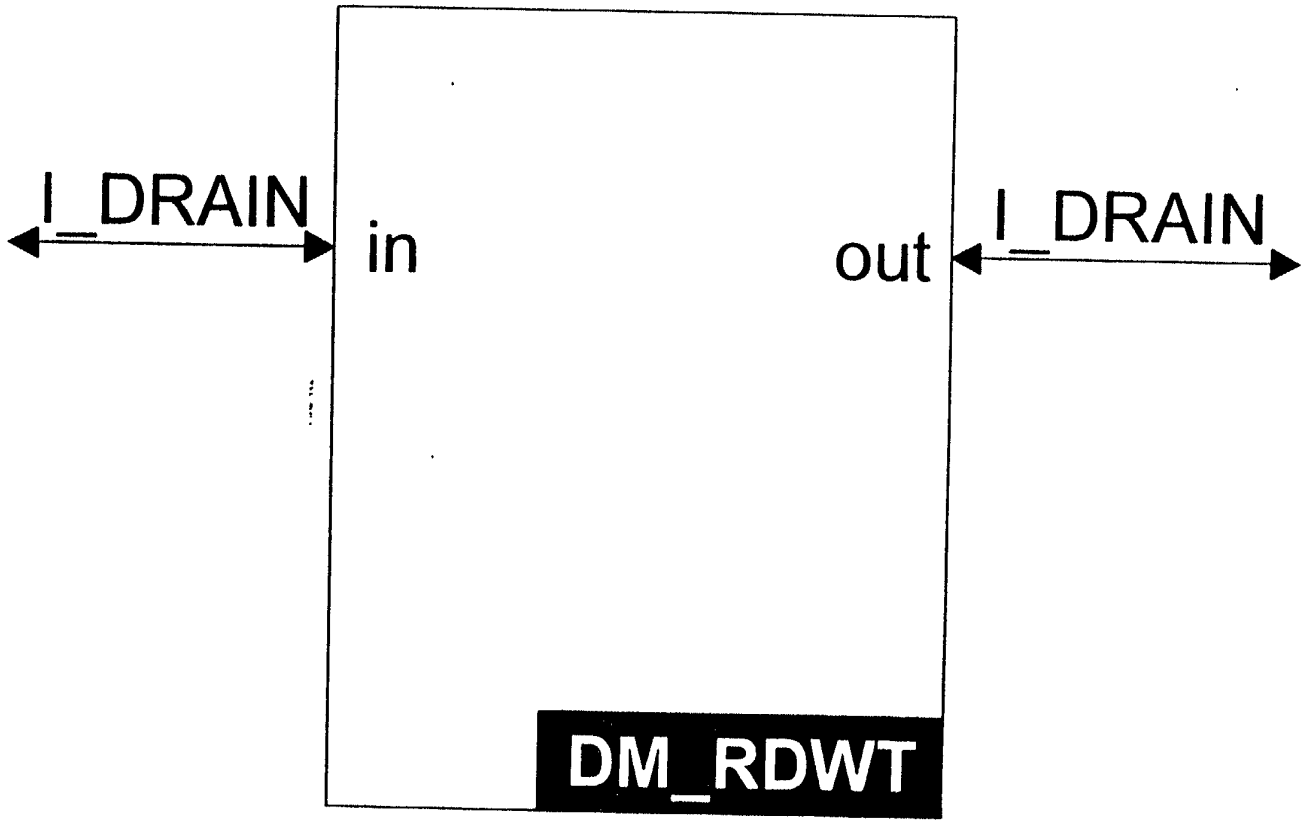


Fig. 100

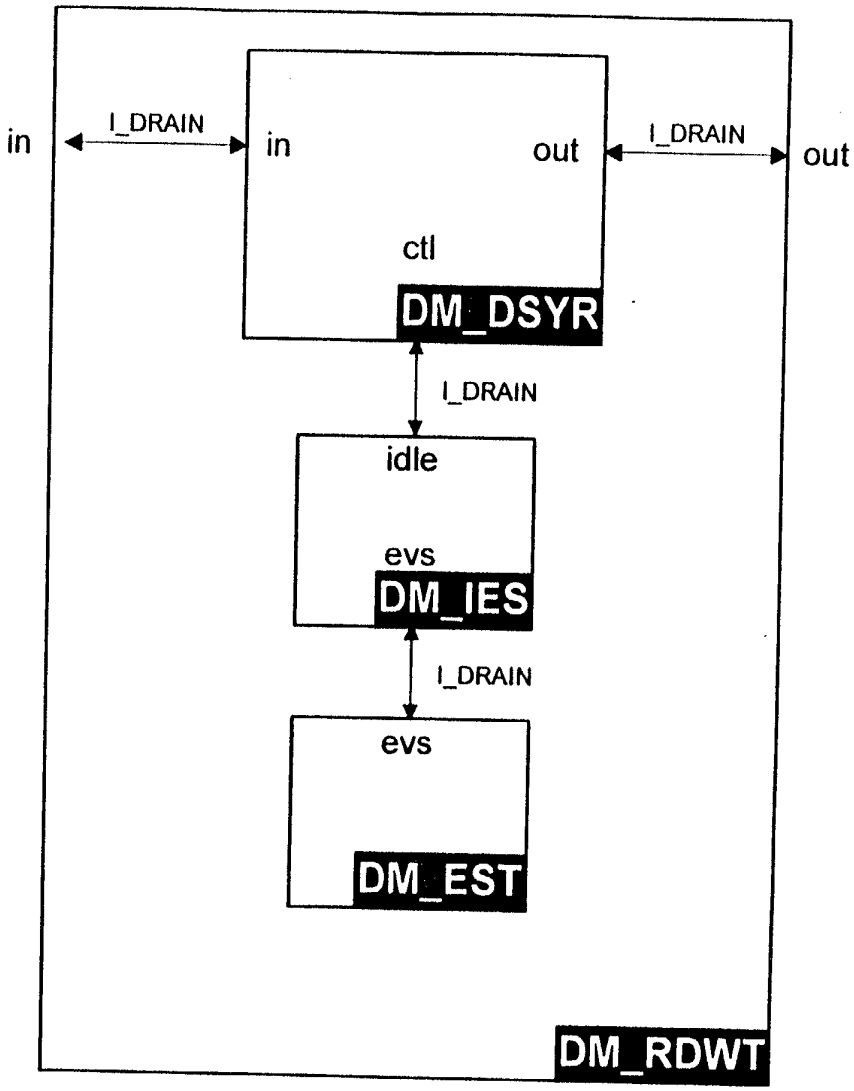

in
I_DRAIN
in
out
I_DRAIN
out
ctl
DM_DSYR
I_DRAIN
idle
evs
DM_IES
I_DRAIN
evs
DM_EST
DM_RDWT

Fig. 101

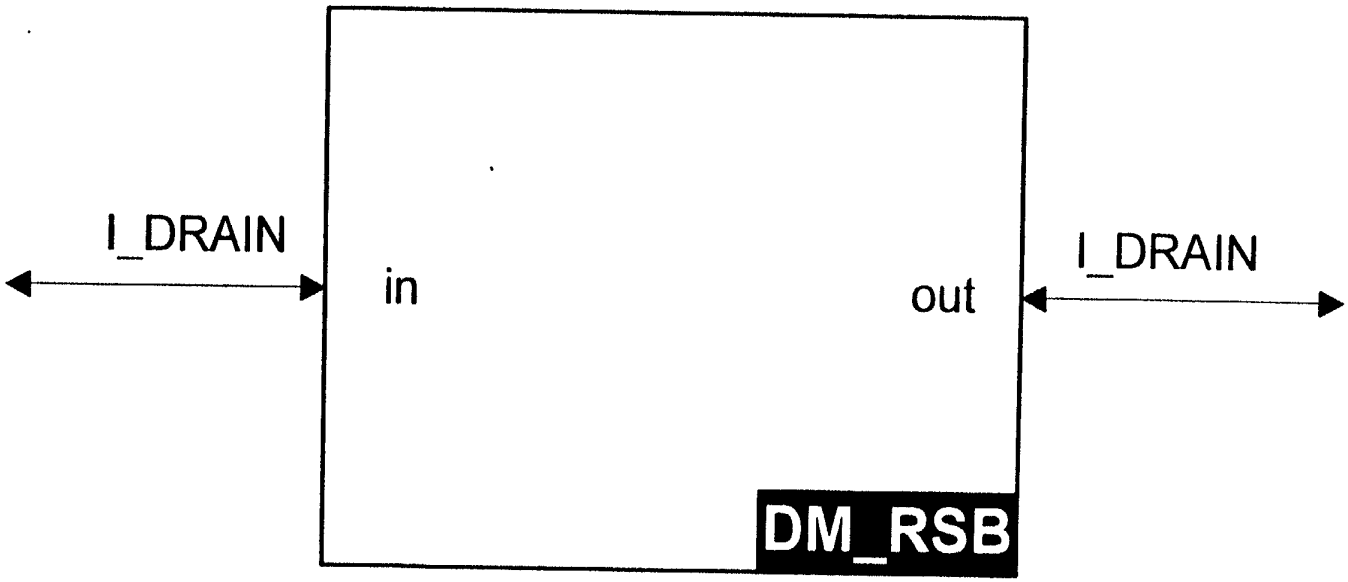


Fig. 102

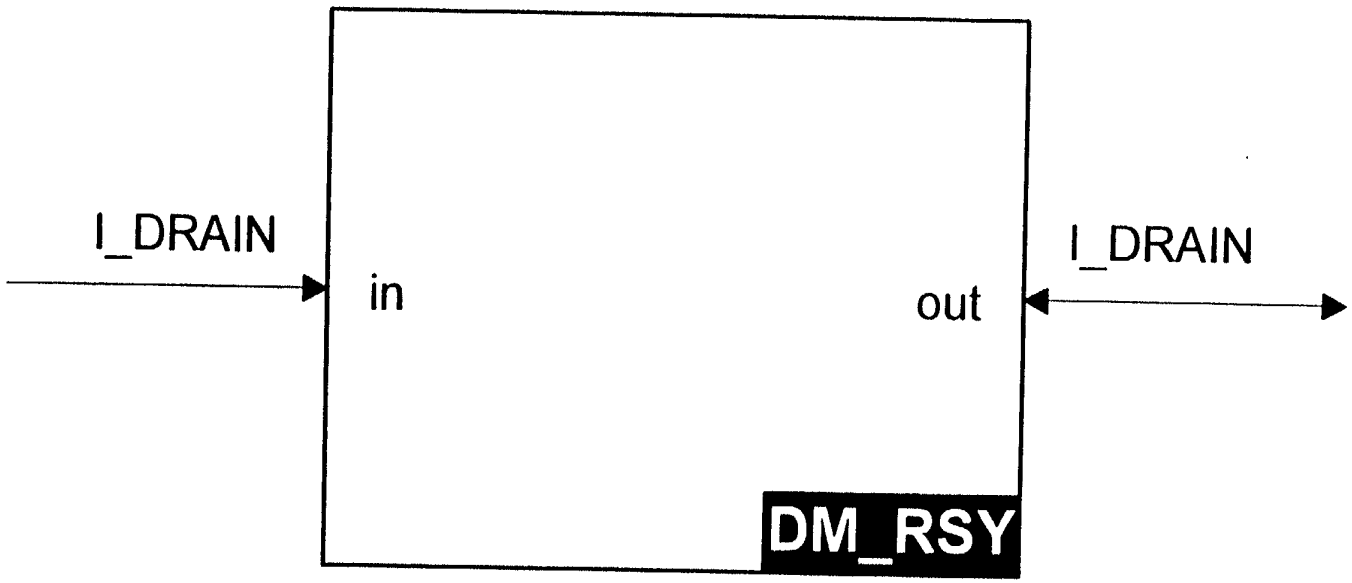


Fig. 103

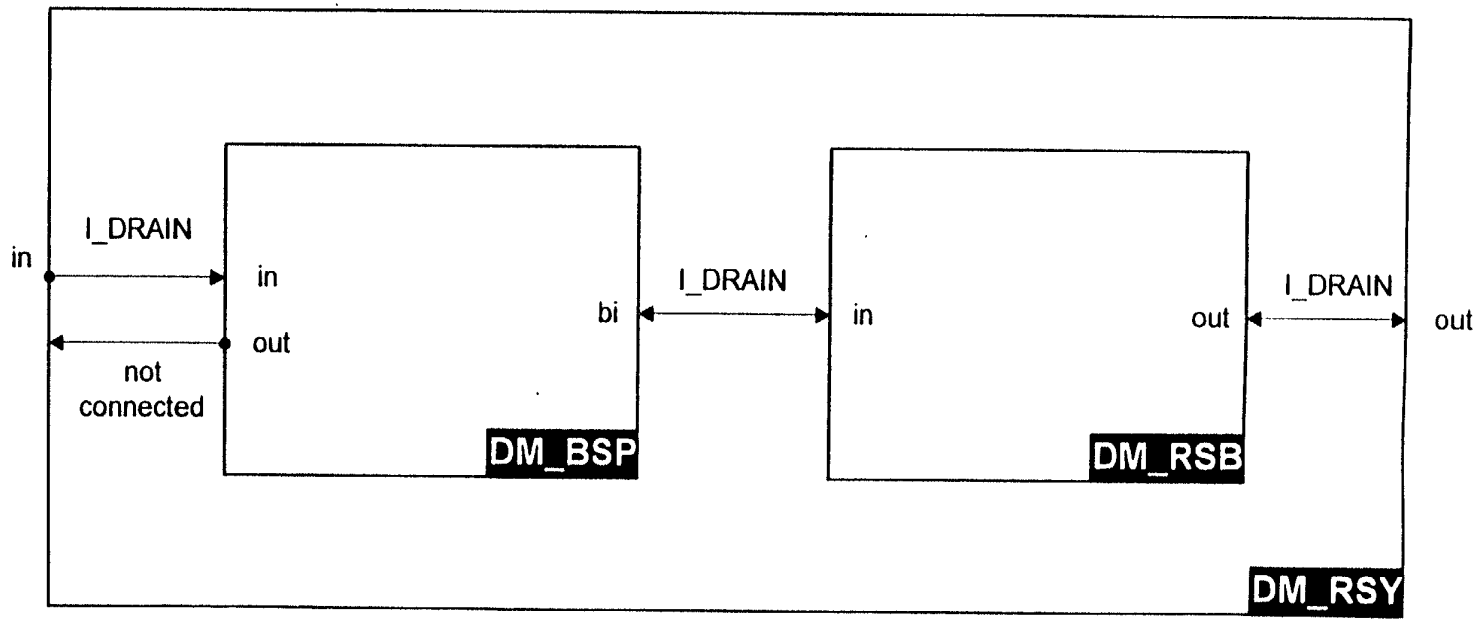

in
I_DRAIN
not
connected
in
out
DM_BSP
bi
I_DRAIN
in
out
DM_RSB
I_DRAIN
out
DM_RSY

Fig. 104

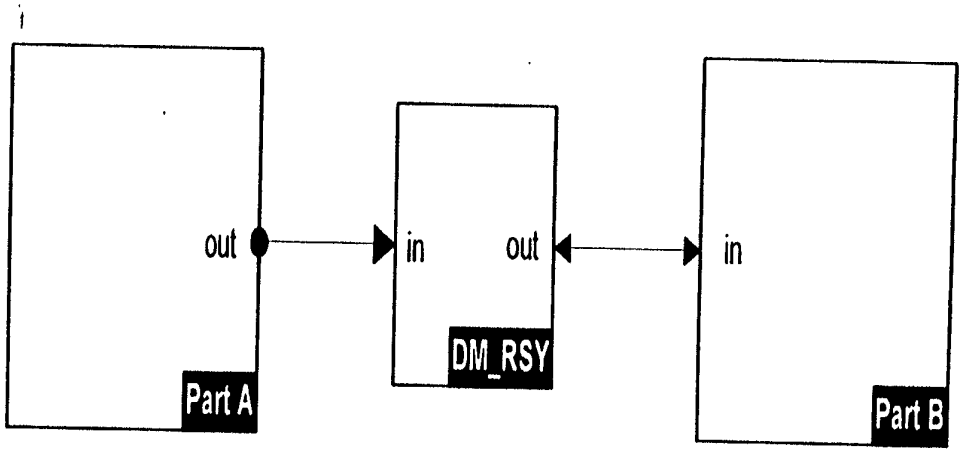


Fig. 105

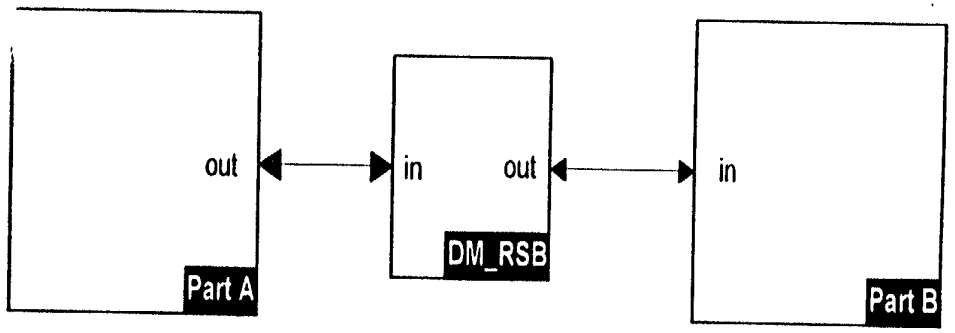


Fig. 106

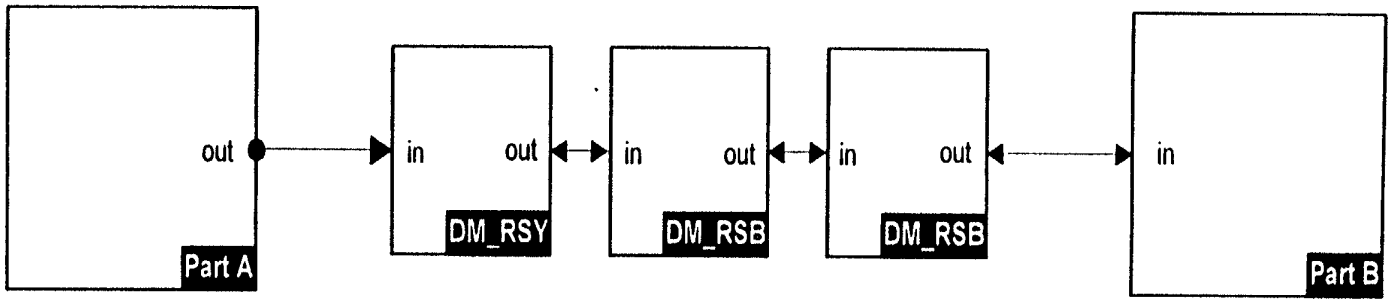


Fig. 107

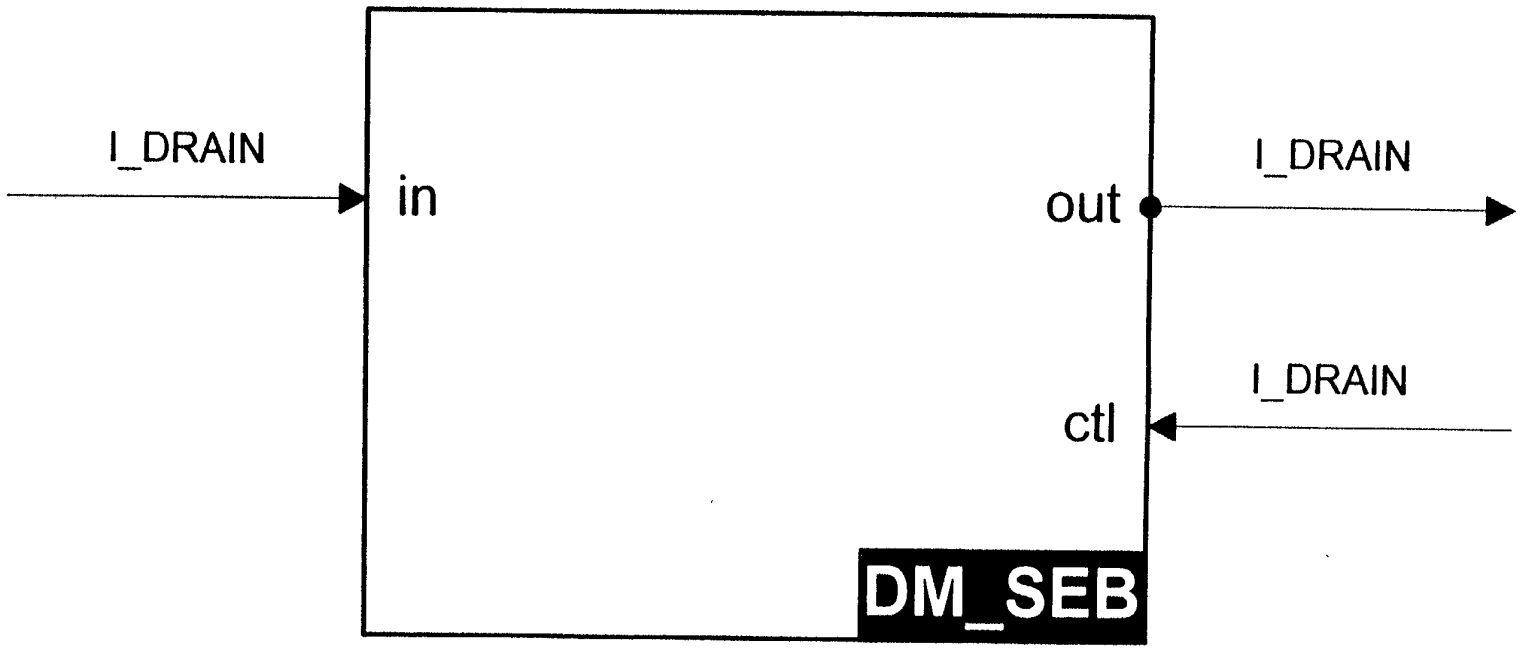


Fig. 108

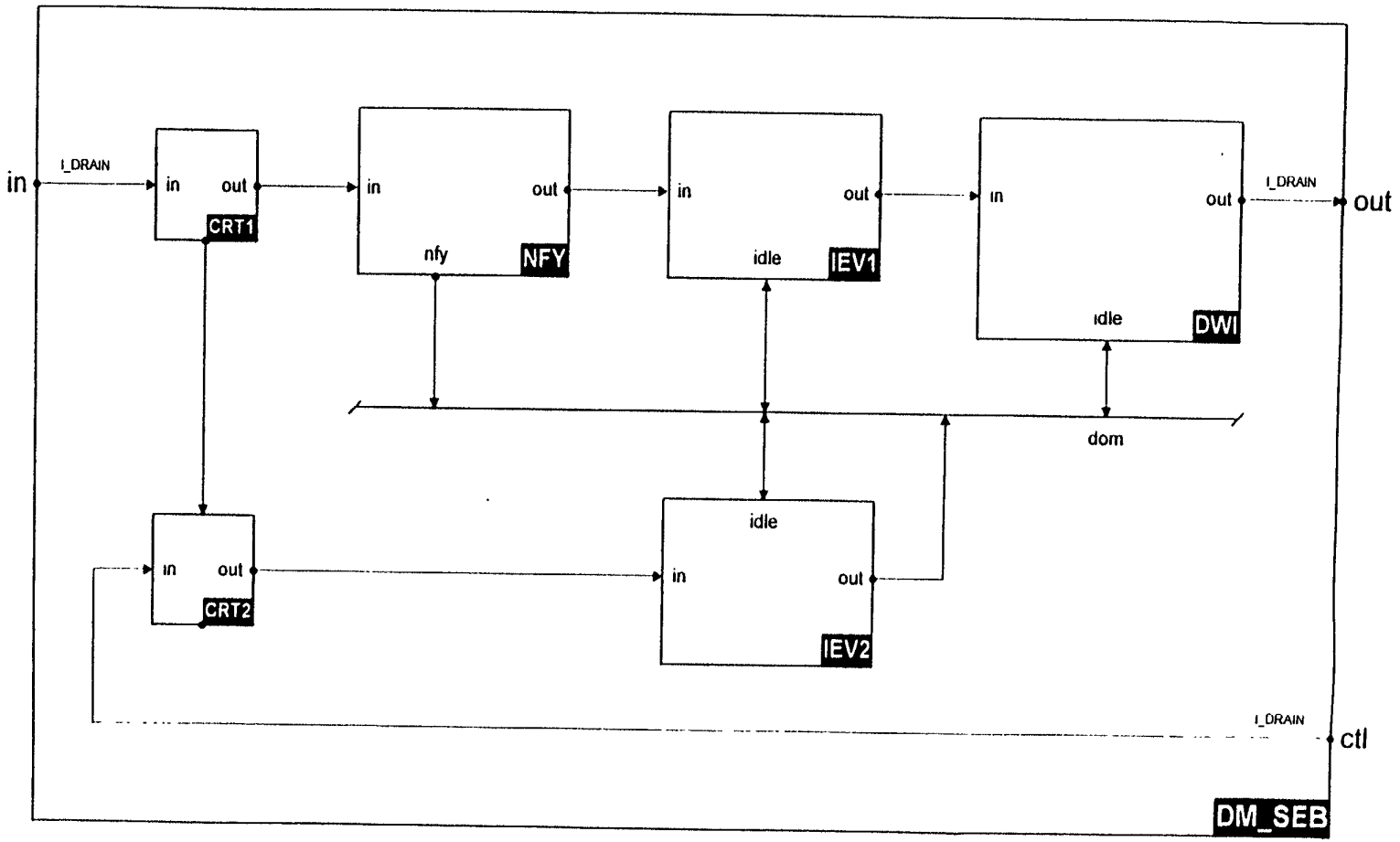

in
I_DRAIN
in
out
CRT1
in
out
nfy
NFY
in
out
idle
IEV1
in
out
idle
DWI
I_DRAIN
out
dom
in
out
CRT2
idle
in
out
IEV2
I_DRAIN
ctl
DM_SEB

Fig. 109

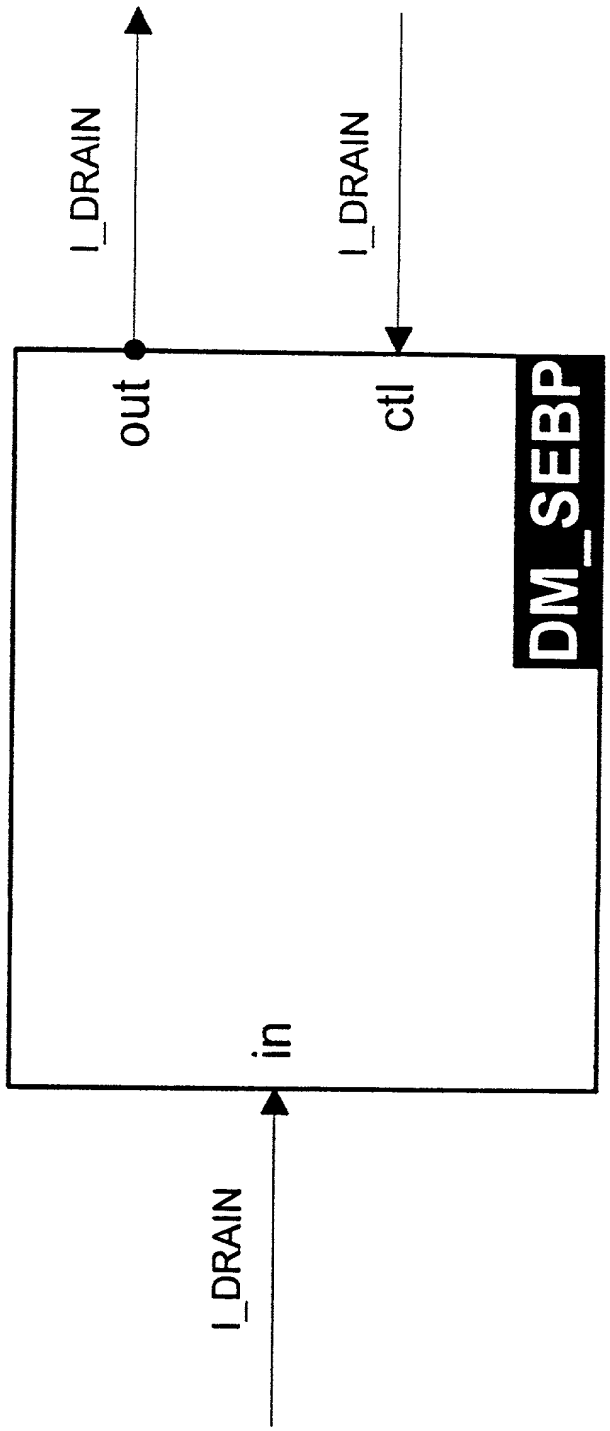


Fig. 110

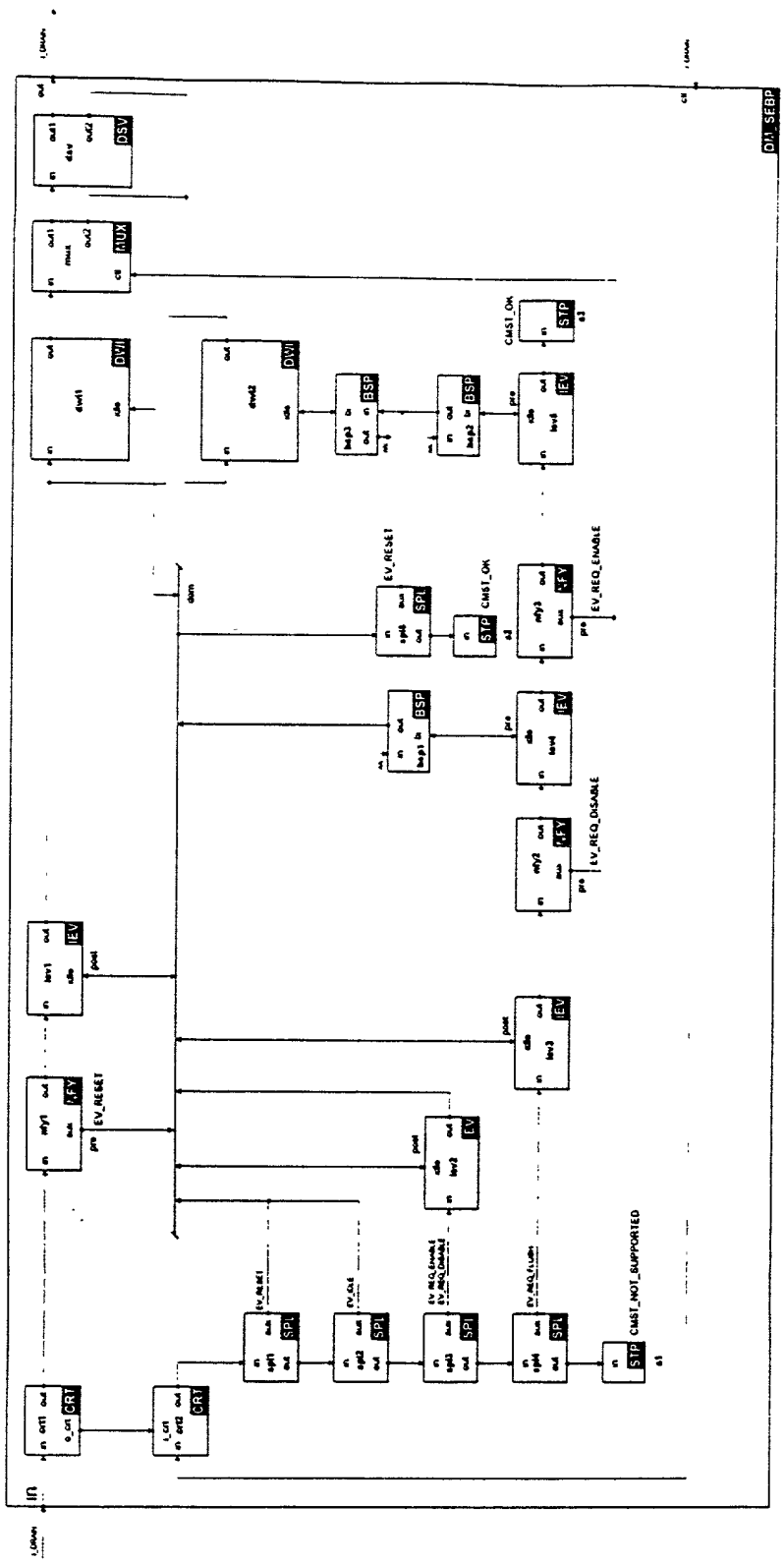


Fig. 111

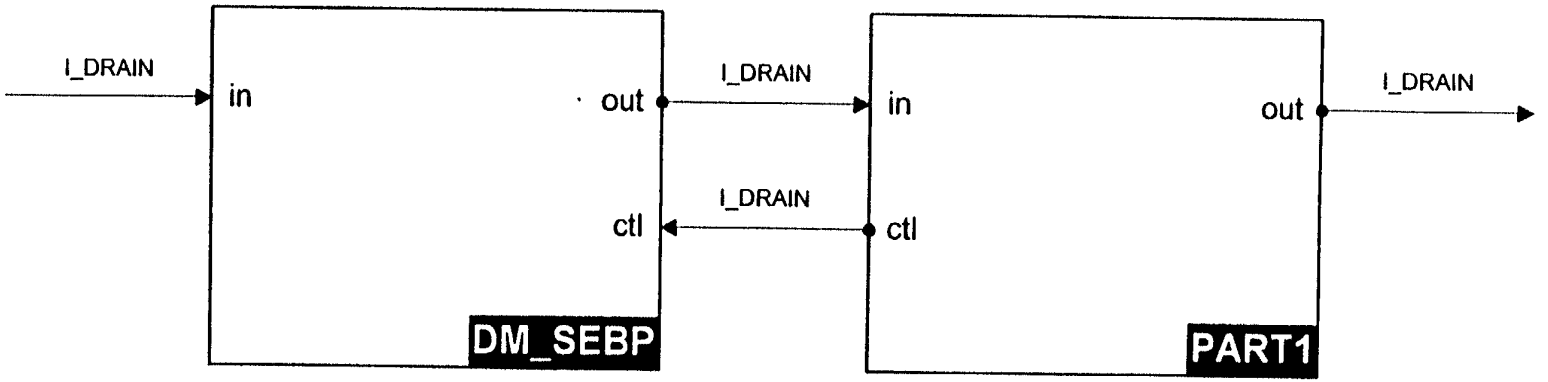

I_DRAIN
in
out
I_DRAIN
in
out
I_DRAIN
I_DRAIN
ctl
ctl
DM_SEBP
PART1

Fig. 112

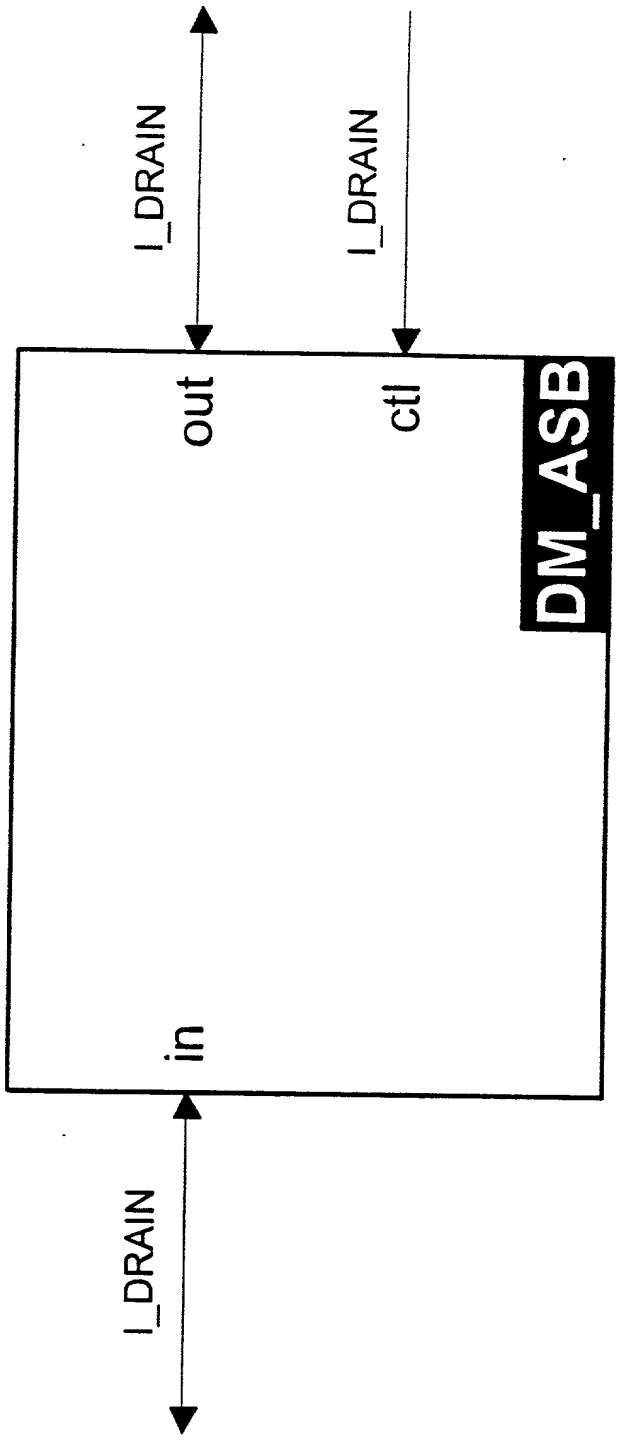


Fig. 113

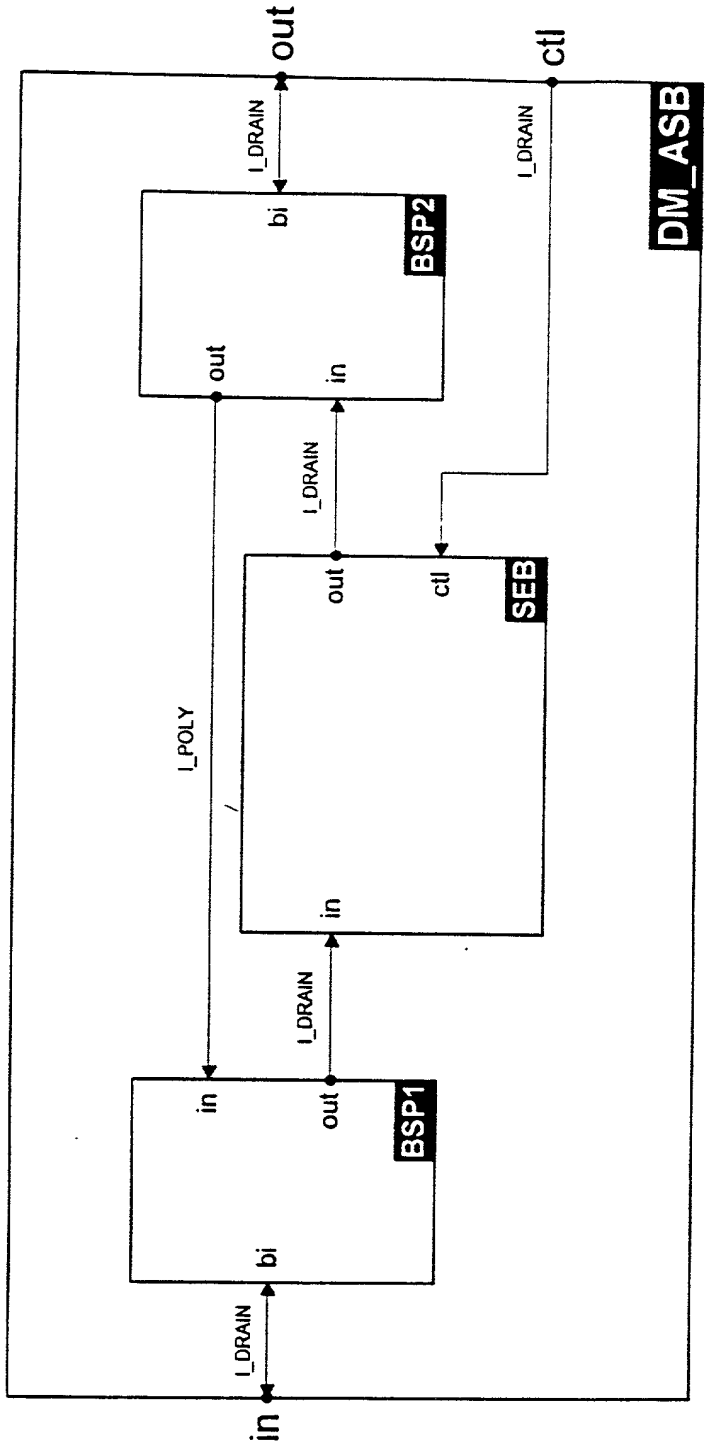

out
ctl
DM_ASB
I_DRAIN
I_DRAIN
bi
BSP2
out
in
I_DRAIN
out
ctl
SEB
I_POLY
in
I_DRAIN
in
out
BSP1
bi
I_DRAIN
in

Fig. 114

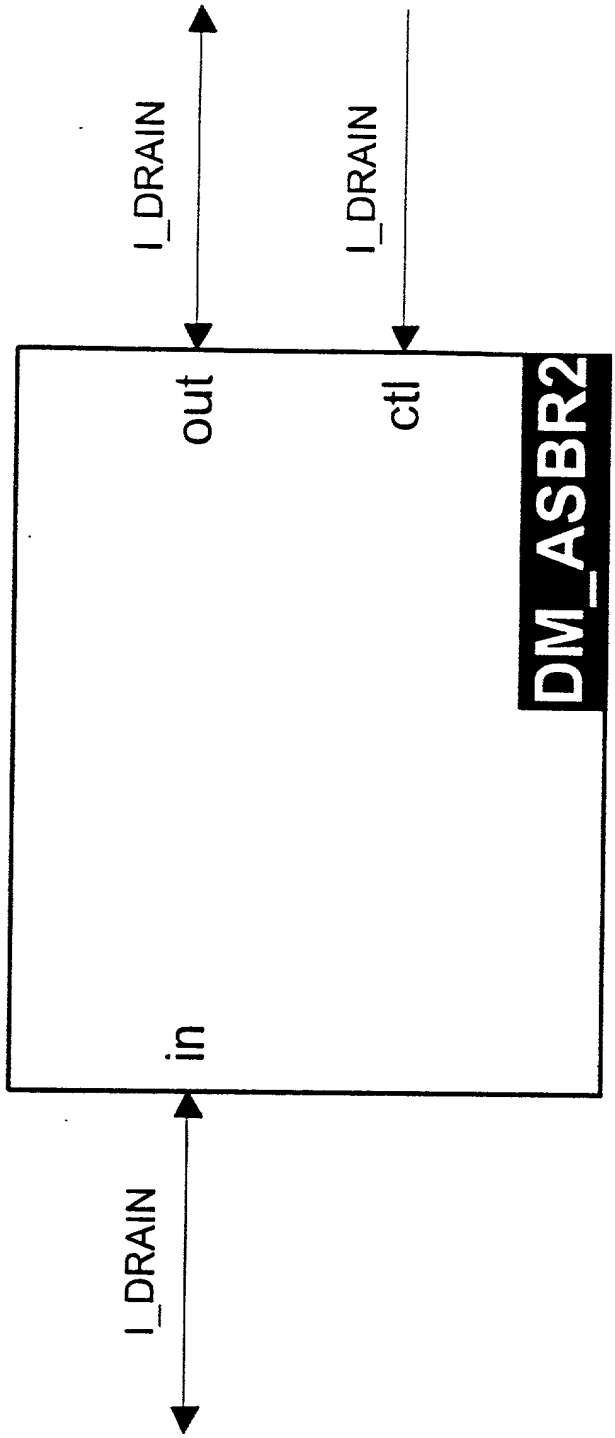


Fig. 115

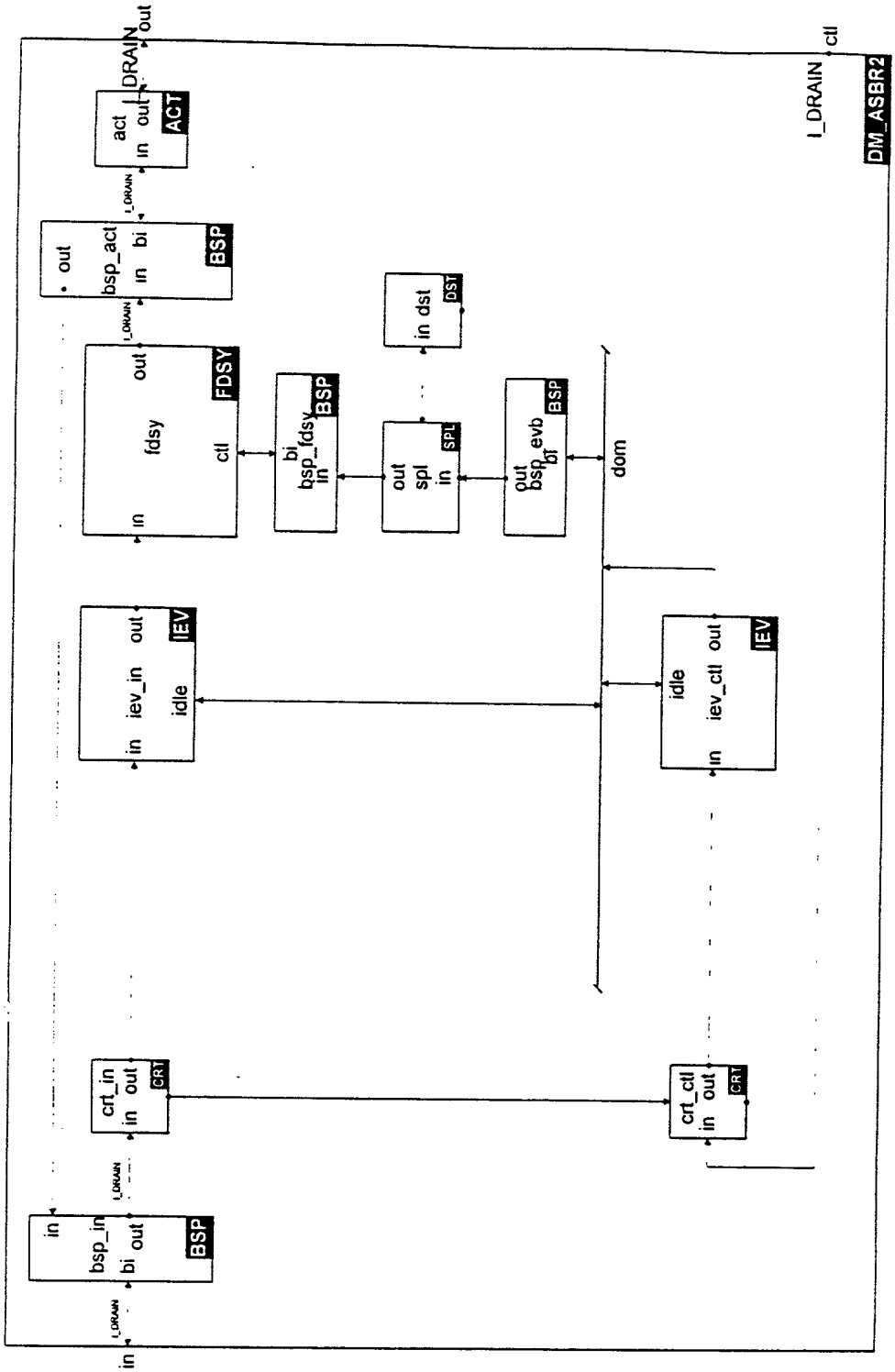

DM_ASBR2
I_DRAIN
ctl
out
DRAIN
act
in out
ACT
I_DRAIN
out
bsp_act
in bi
BSP
I_DRAIN
out
fdsy
ctl
in
FDSY
bi
bsp_fdsy
in
BSP
in dst
DST
out
spl
in
SPL
out
bsp_evb
bi
BSP
dom
in
iev_in
idle
out
IEV
idle
iev_ctl
in
out
IEV
crt_in
in out
CRT
crt_ctl
in out
CRT
I_DRAIN
in
bsp_in
bi out
BSP
I_DRAIN
in

Fig. 116

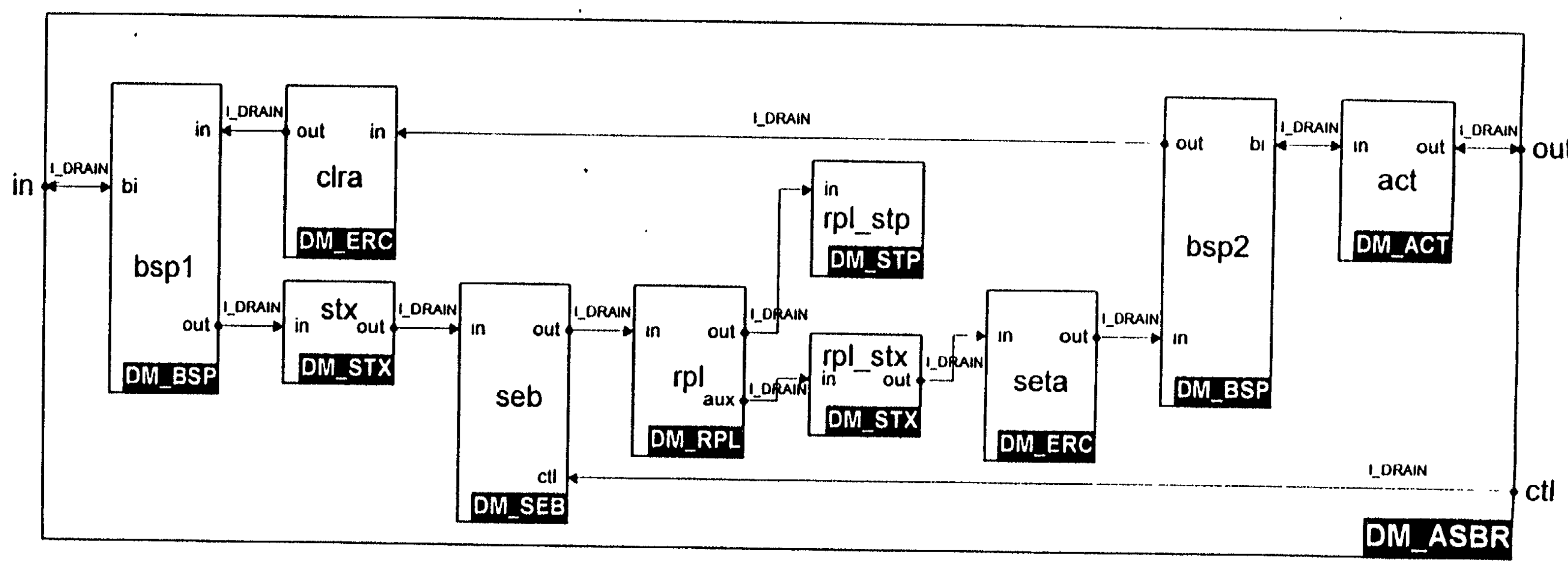

in
out
ctl
I_DRAIN
bsp1
bi
in
out
DM_BSP
clra
out
in
DM_ERC
stx
in
out
DM_STX
seb
in
out
ctl
DM_SEB
rpl
in
out
aux
DM_RPL
rpl_stp
in
DM_STP
rpl_stx
in
out
DM_STX
seta
in
out
DM_ERC
bsp2
out
bi
in
DM_BSP
act
in
out
DM_ACT
DM_ASBR

Fig. 117

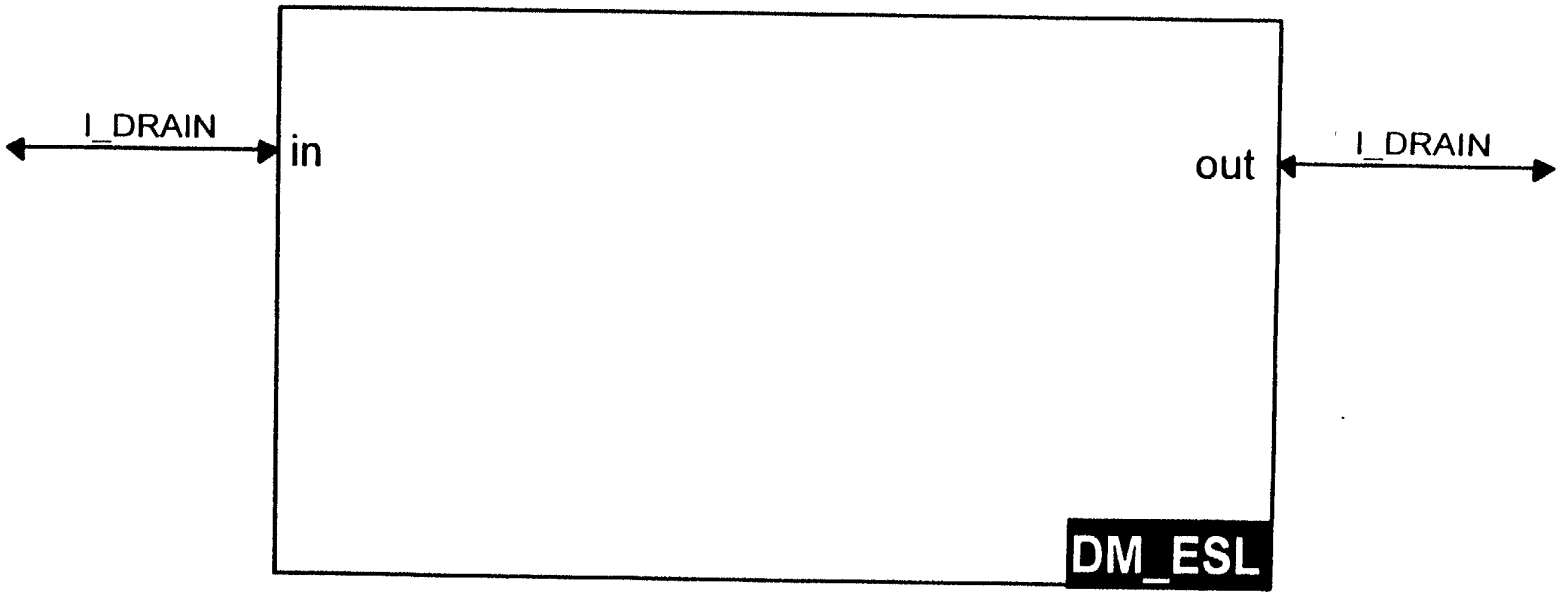


Fig. 118

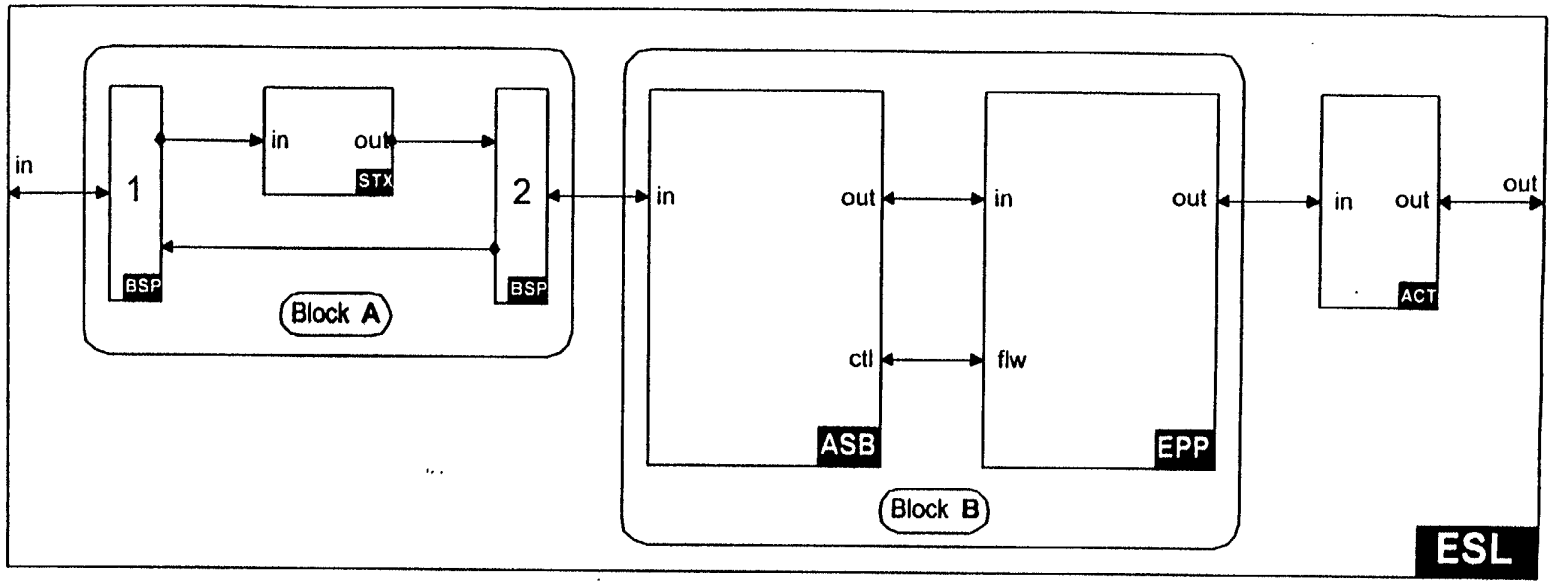

in
1
BSP
in
out
STX
2
BSP
Block A
in
out
ctl
ASB
in
out
flw
EPP
Block B
in
out
ACT
out
ESL

Fig. 119

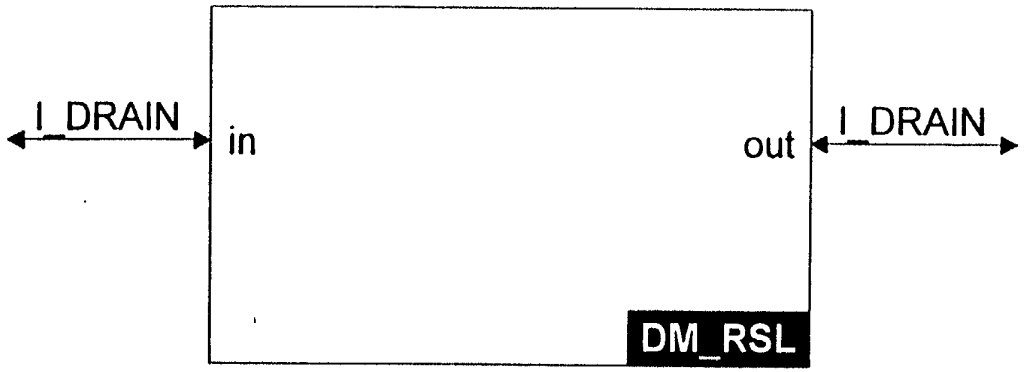
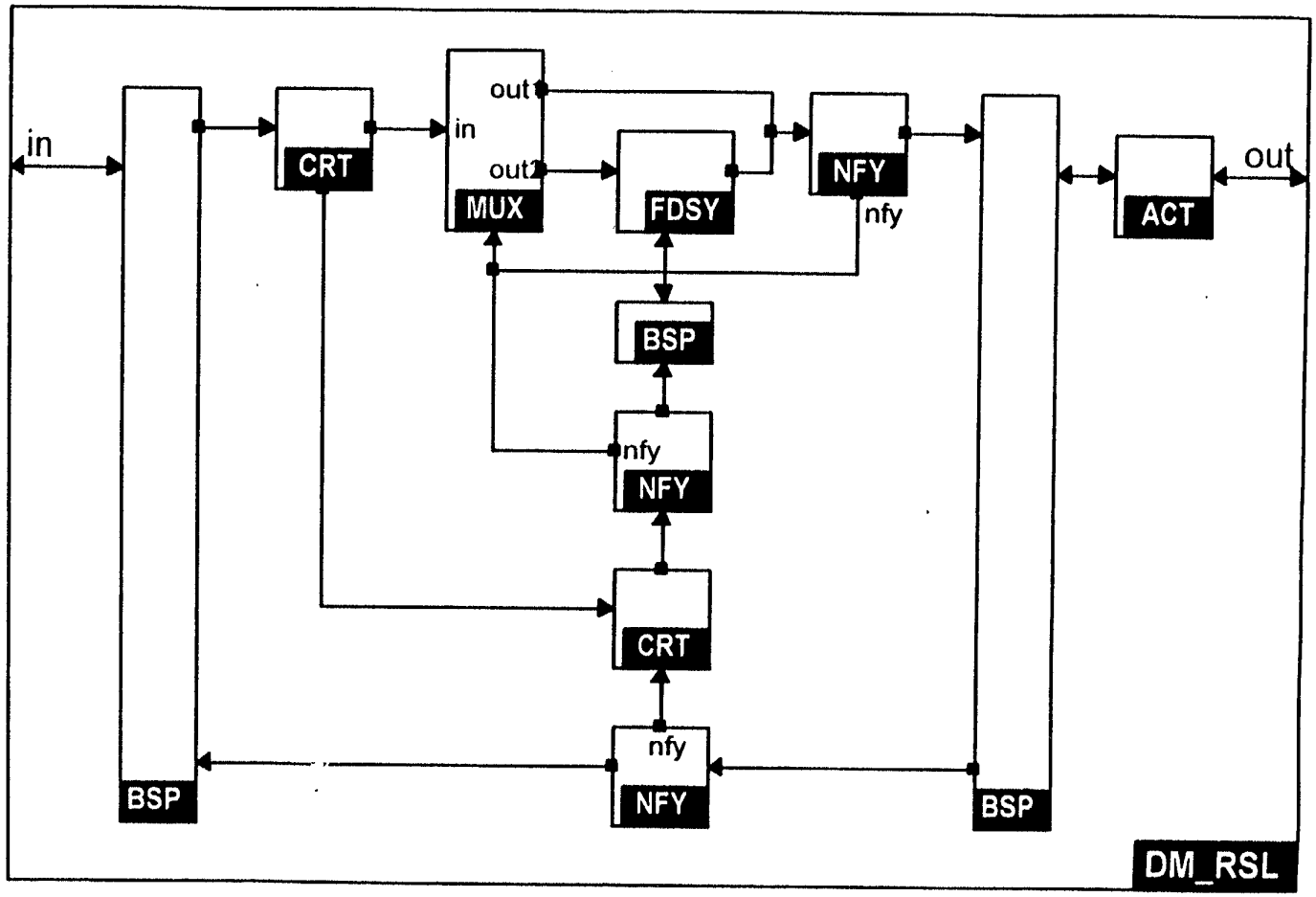


Fig. 120



Note: all connections are I_DRAIN type

Fig. 121

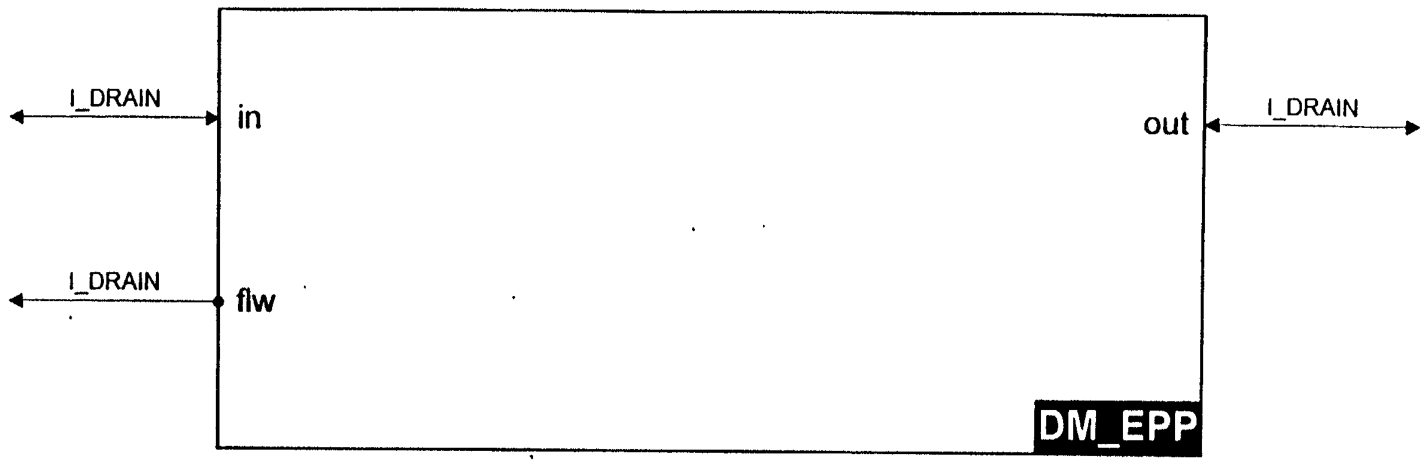


Fig. 122

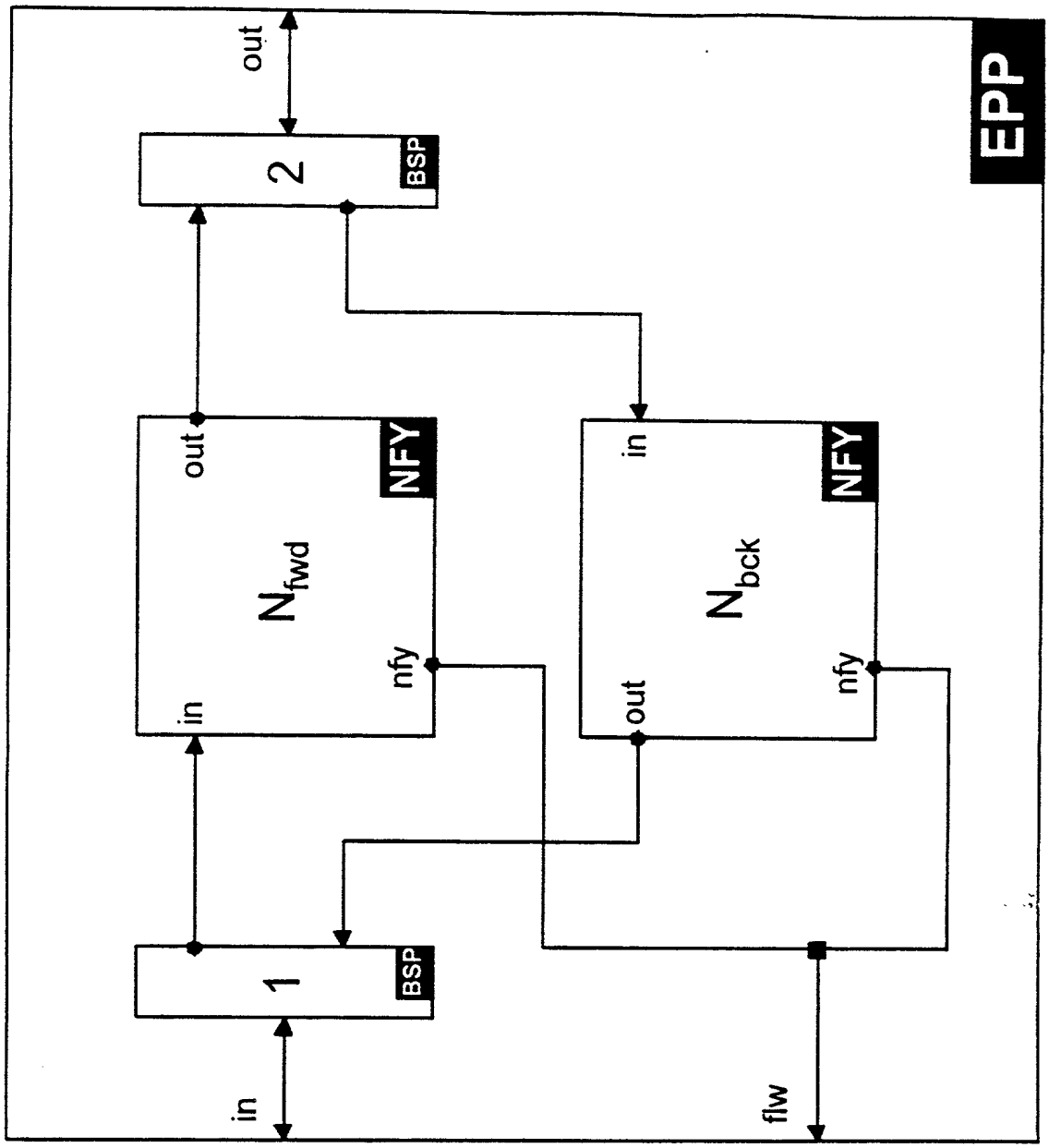

EPP
out
2
BSP
out
NFY
N_{fwd}
nfy
in
in
NFY
N_{bck}
nfy
out
in
1
BSP
in
flw

Fig. 123

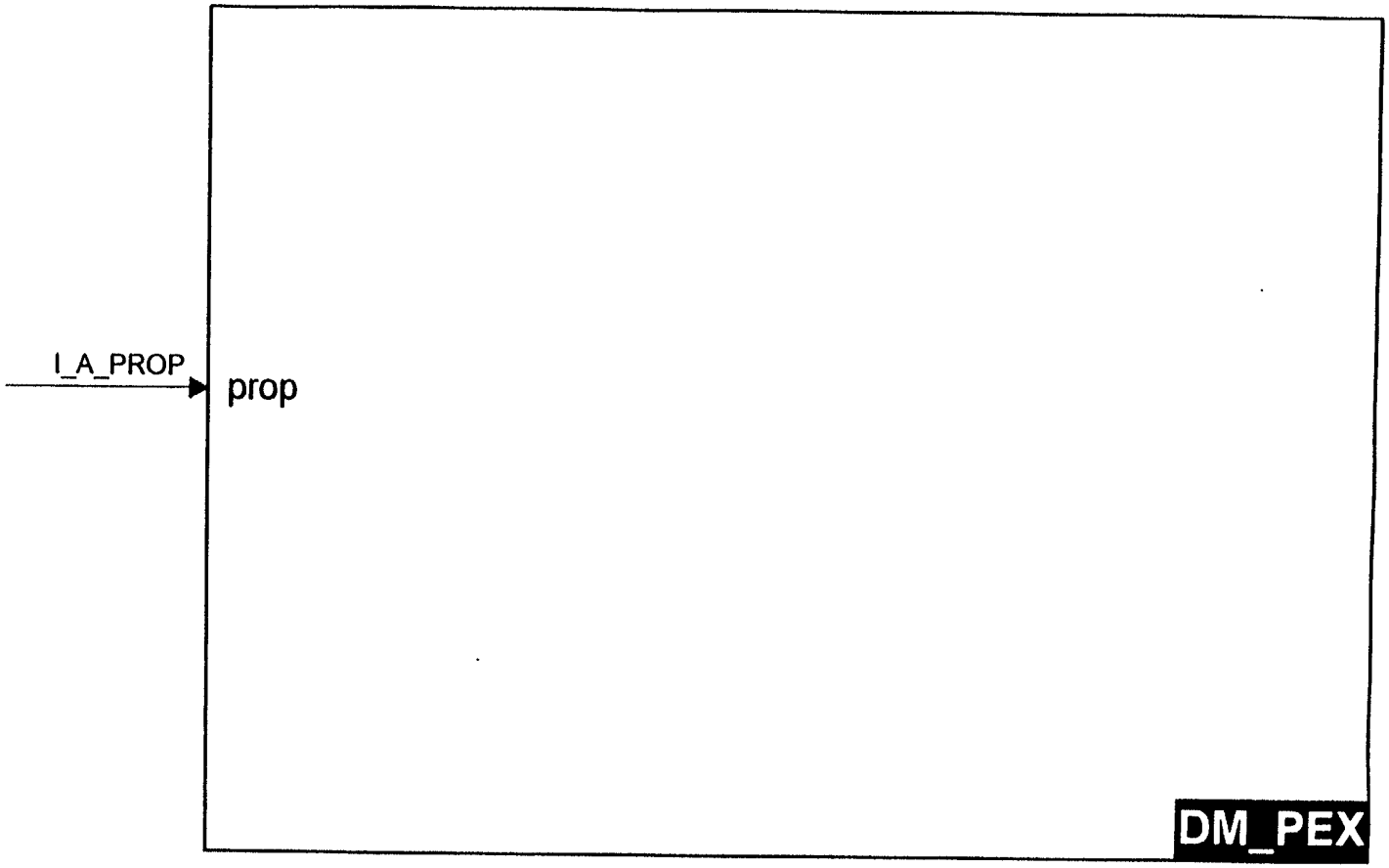


Fig. 124

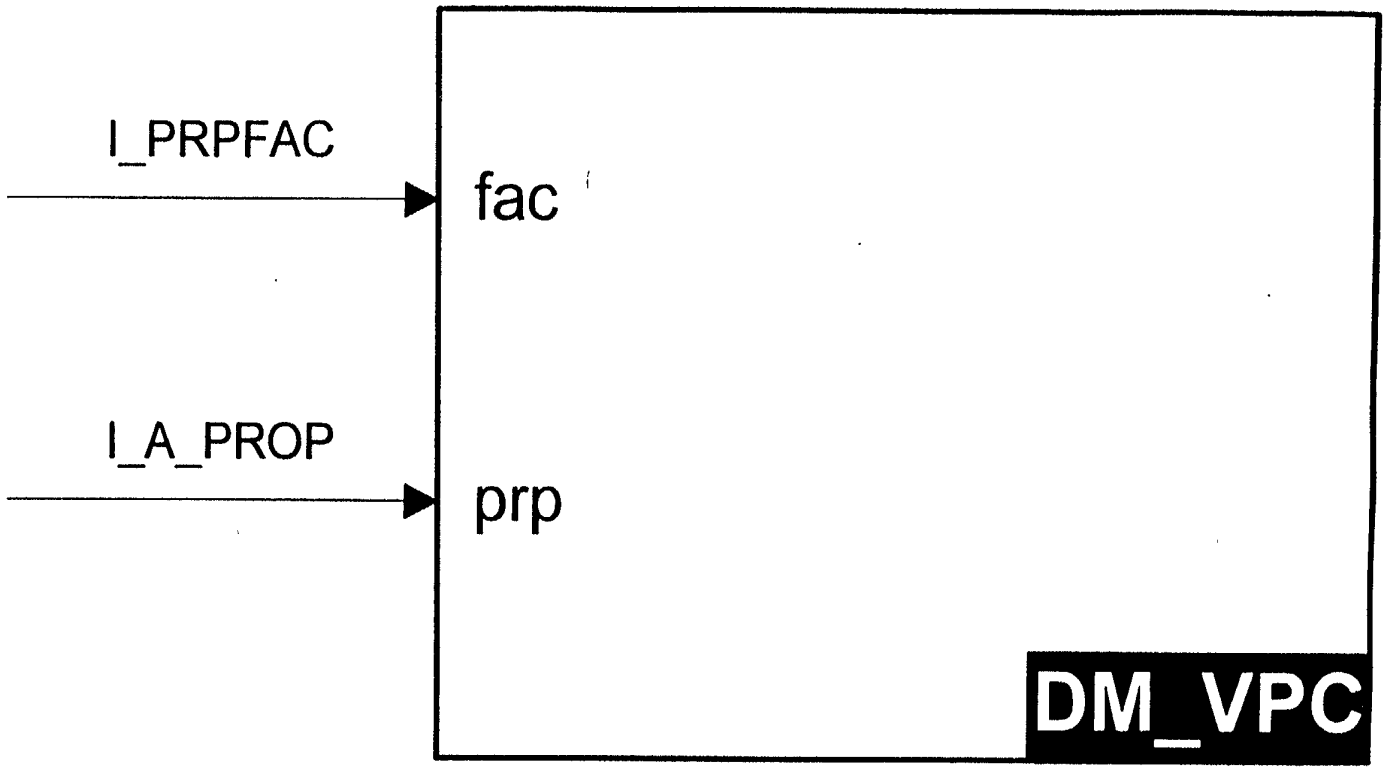


Fig. 125

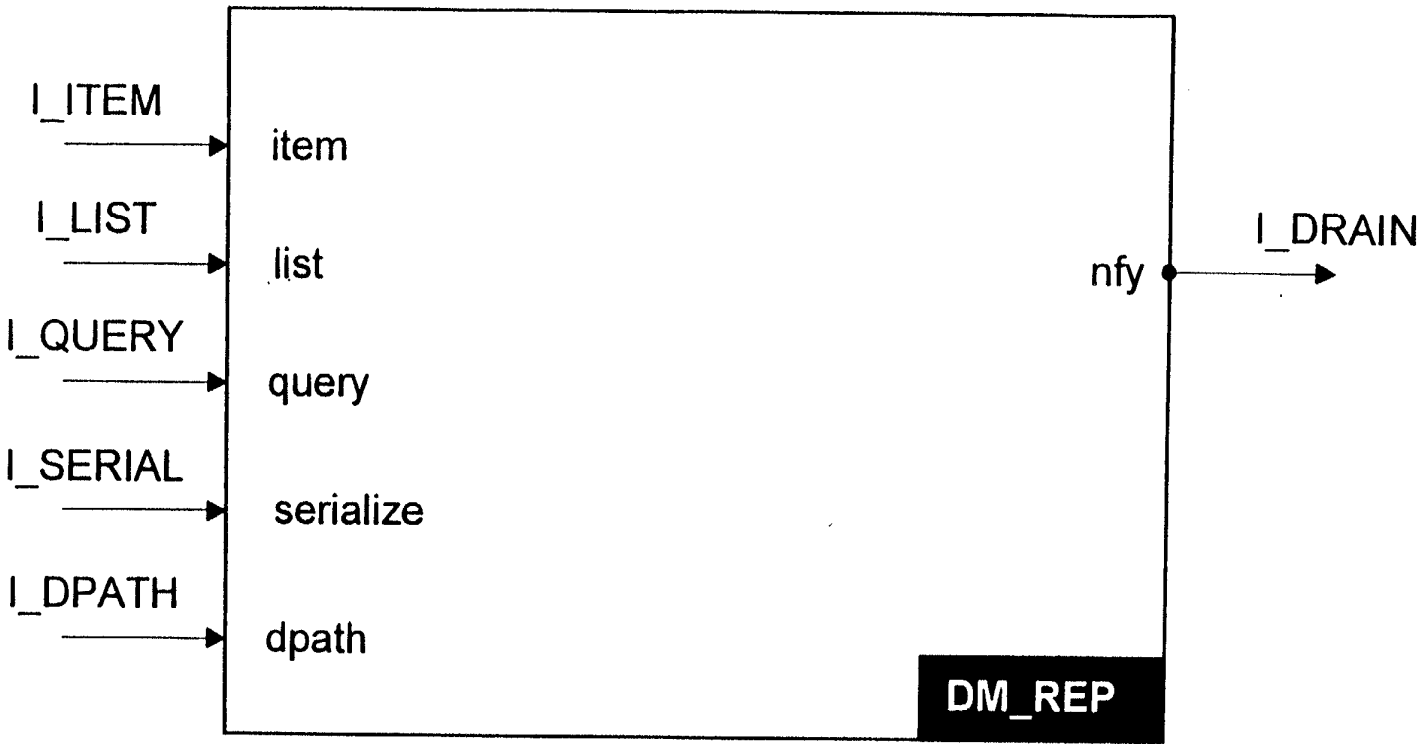
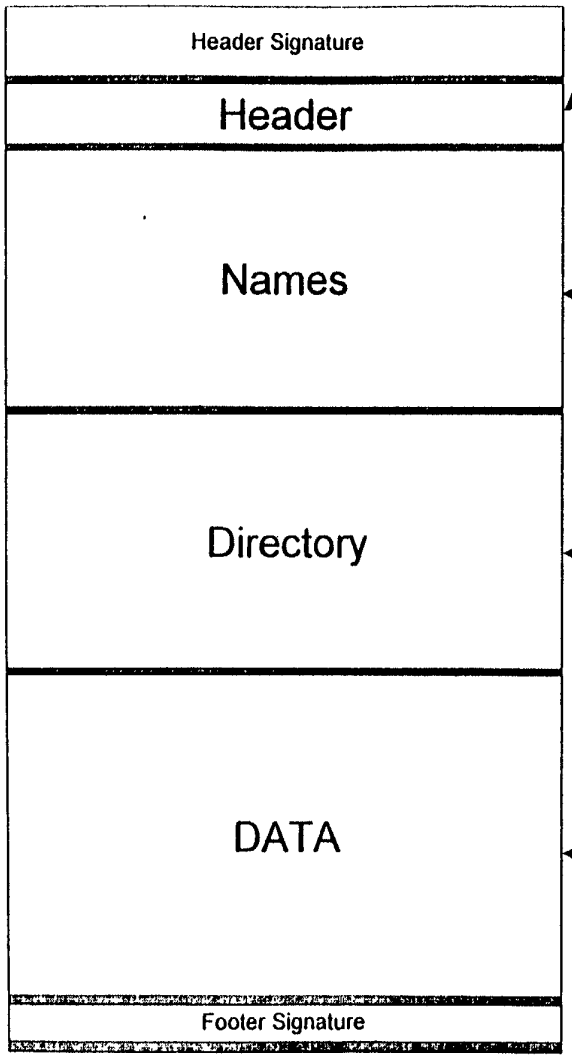

I_ITEM
item
I_LIST
list
I_QUERY
query
I_SERIAL
serialize
I_DPATH
dpath
nfy
I_DRAIN
DM_REP

Fig. 126




```
DWORD max_levels;       // max. number of path levels
DWORD name_stg;         // name storage (max. name len + 1 for '\0')
DWORD pel_sz;           // size of pel, [bytes]
DWORD name_entry_sz;    // size of name entry, [bytes]
DWORD n_names;          // number of names in file
DWORD entry_sz;         // size of directory entry, [bytes]
DWORD n_entries;        // number of entries in file
DWORD reserved[8];      // for future extensions, must be 0
```

```
[array containing <n_names> items of the following structure: ]
   char        name[32];          // array of names
   _pel        pel;               // path element value
```

```
_pel       pel [16];              // address in path elements
DWORD      len;                   // data length
DWORD      ctx;                   // item context value
WORD       reserved;              // reserved, value is ignored
```

```
[ sequential blocks of data; each of them has variable size length ]
[ according to the directory field <len>                           ]
```

Fig. 127

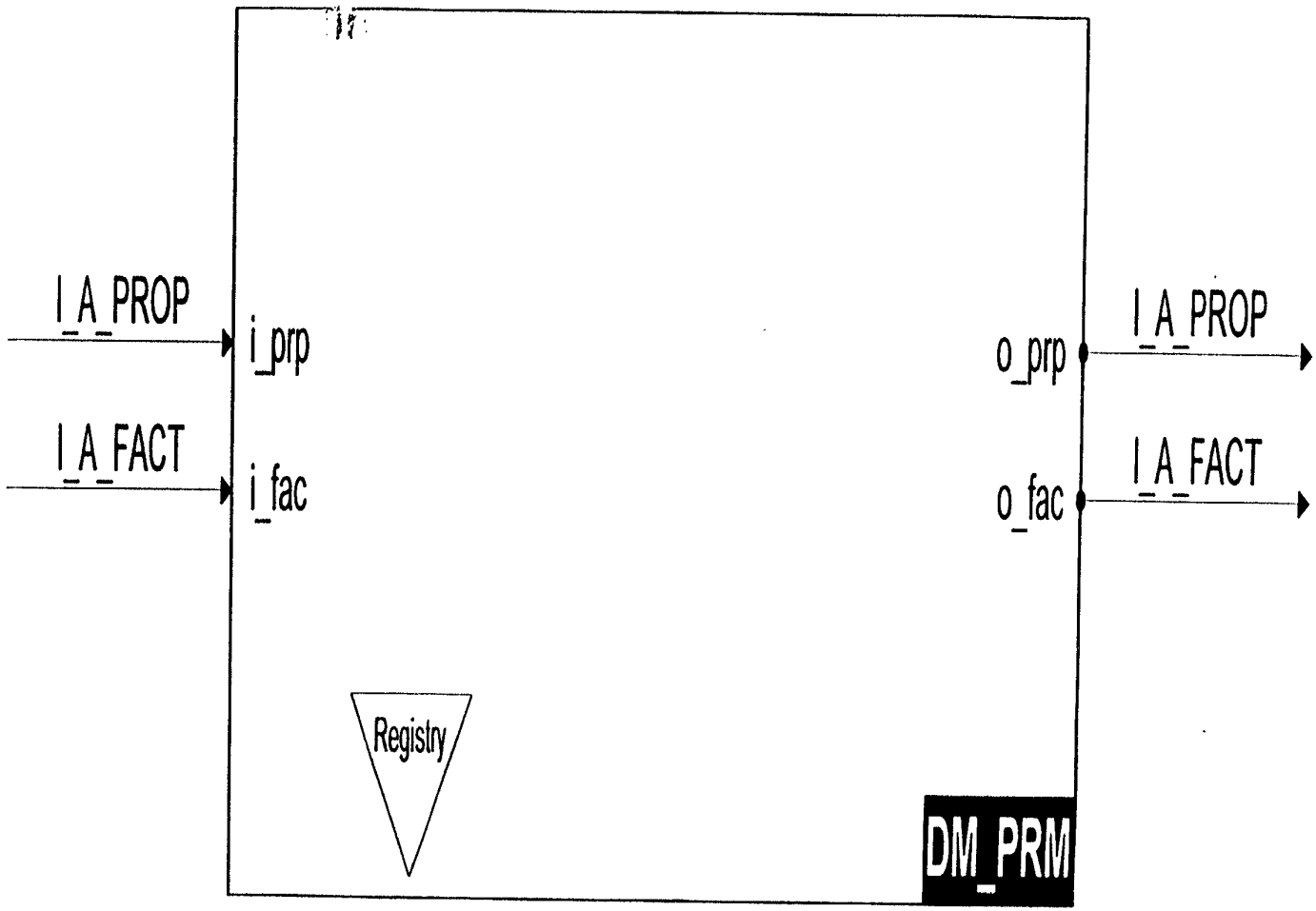

I_A_PROP
i_prp
I_A_FACT
i_fac
o_prp
o_fac
I_A_PROP
I_A_FACT
Registry
DM_PRM

Fig. 128

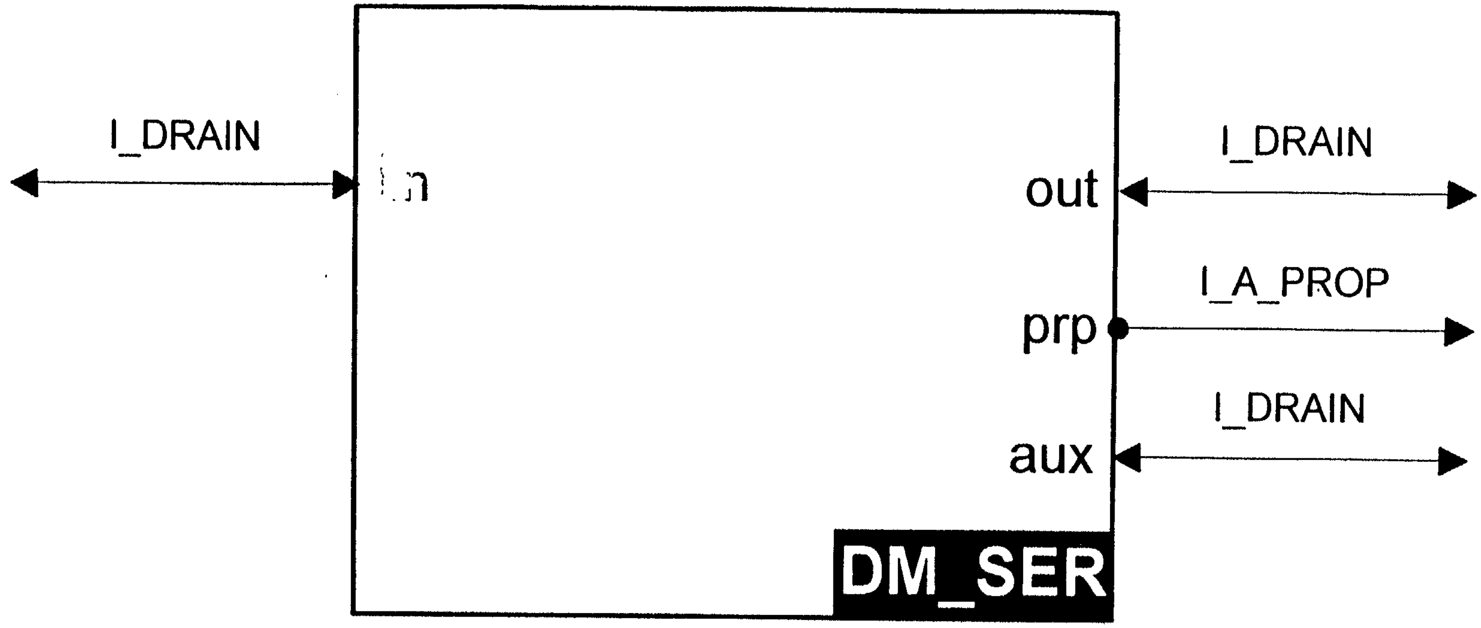


Fig. 129

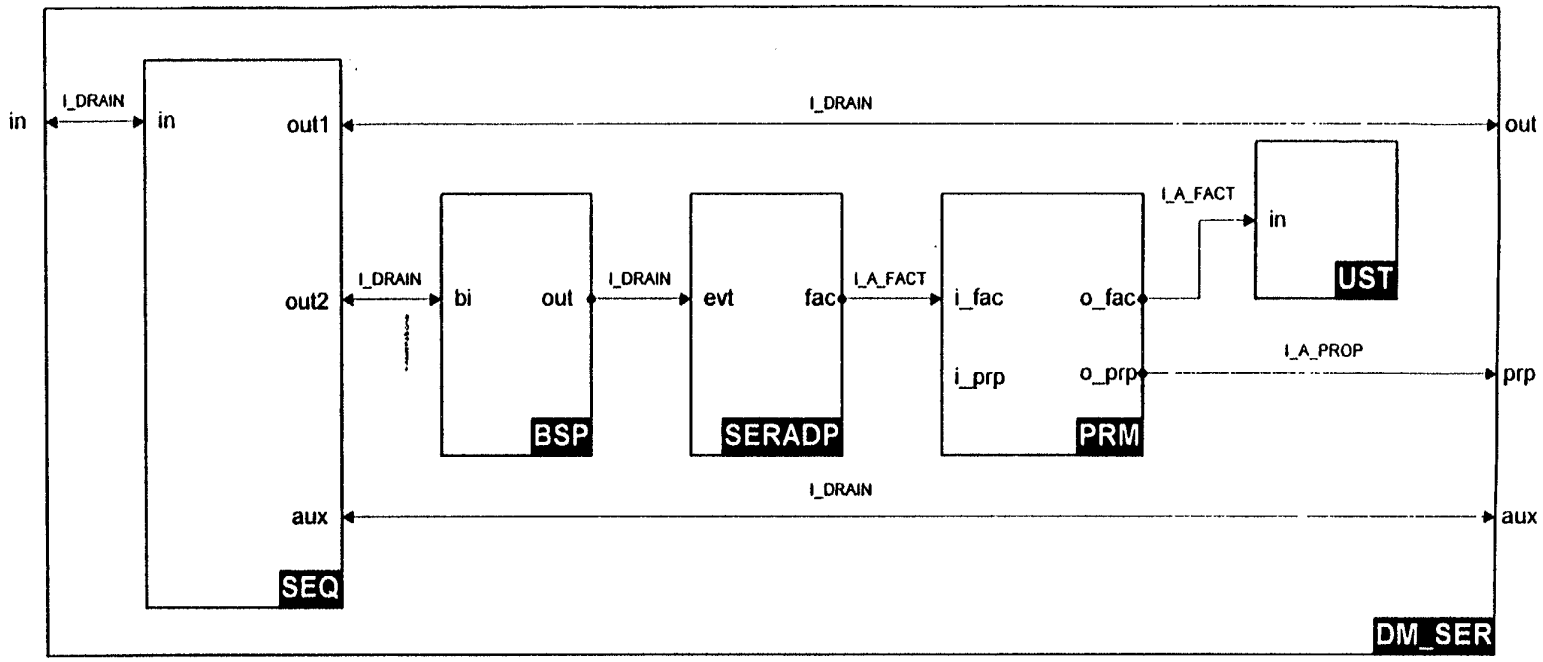

in
I_DRAIN
in
out1
out2
aux
SEQ
I_DRAIN
bi
out
BSP
I_DRAIN
evt
fac
SERADP
I_A_FACT
i_fac
o_fac
i_prp
o_prp
PRM
I_A_FACT
in
UST
I_A_PROP
prp
I_DRAIN
out
I_DRAIN
aux
DM_SER

Fig. 130

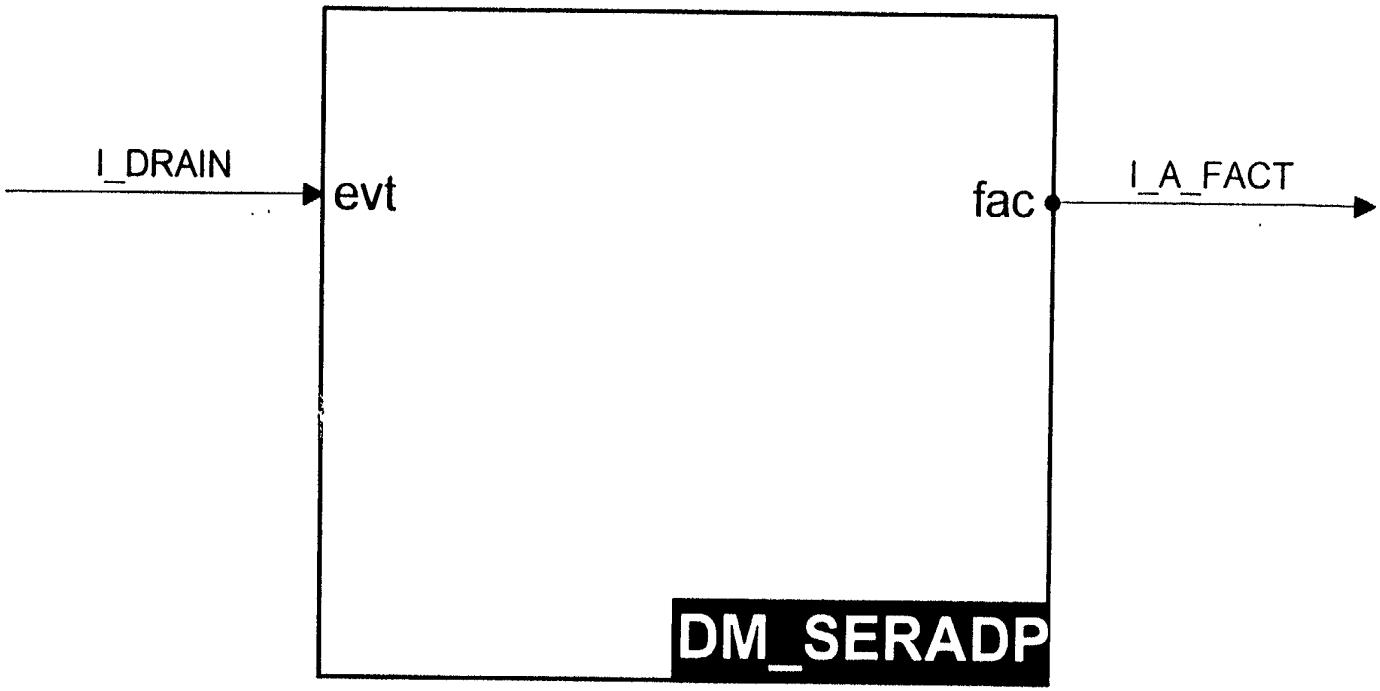


Fig. 131

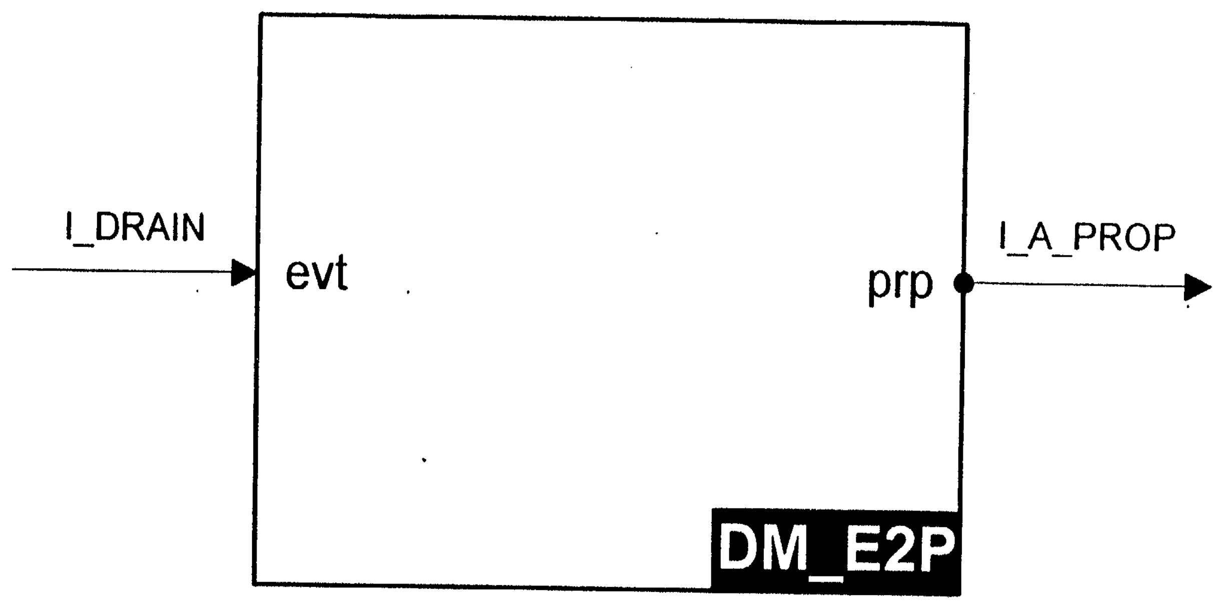


Fig. 132

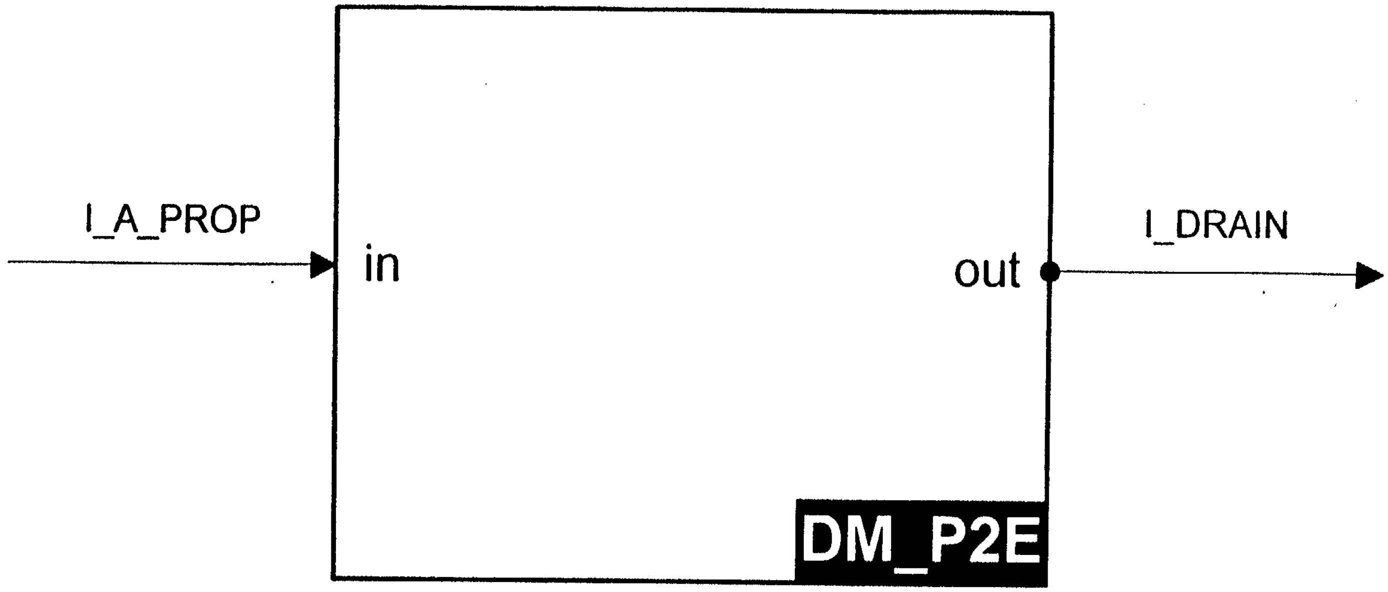


Fig. 133

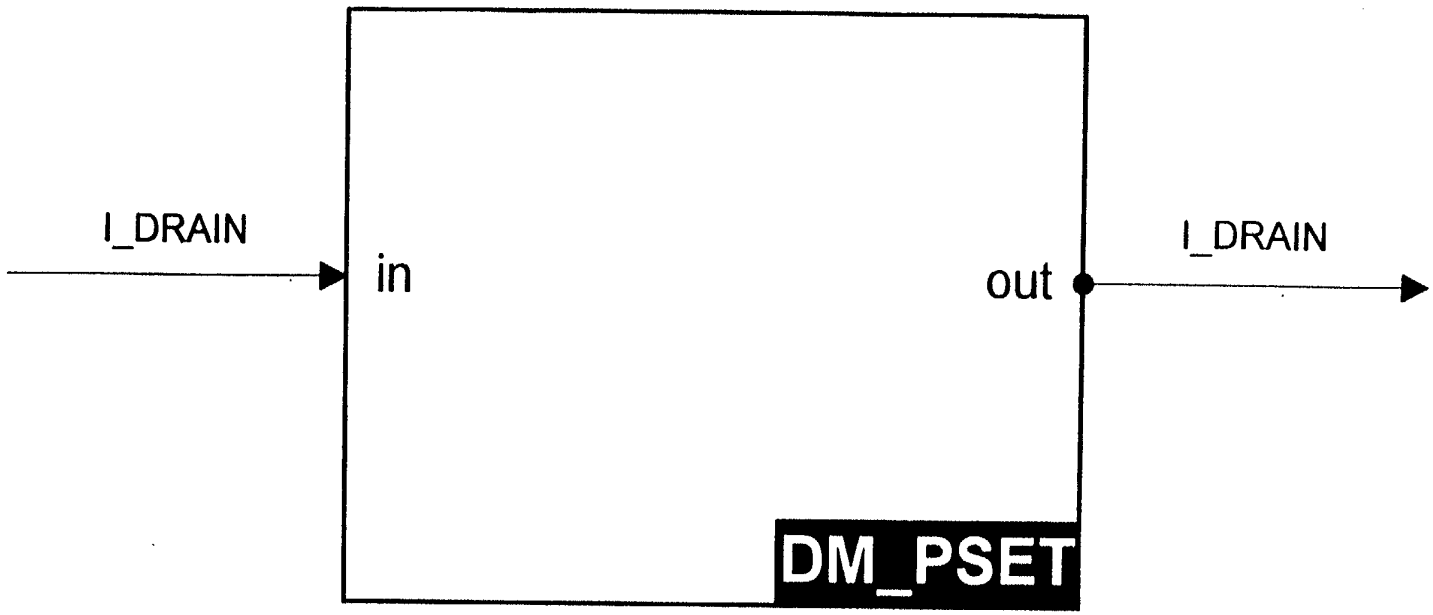


Fig. 134

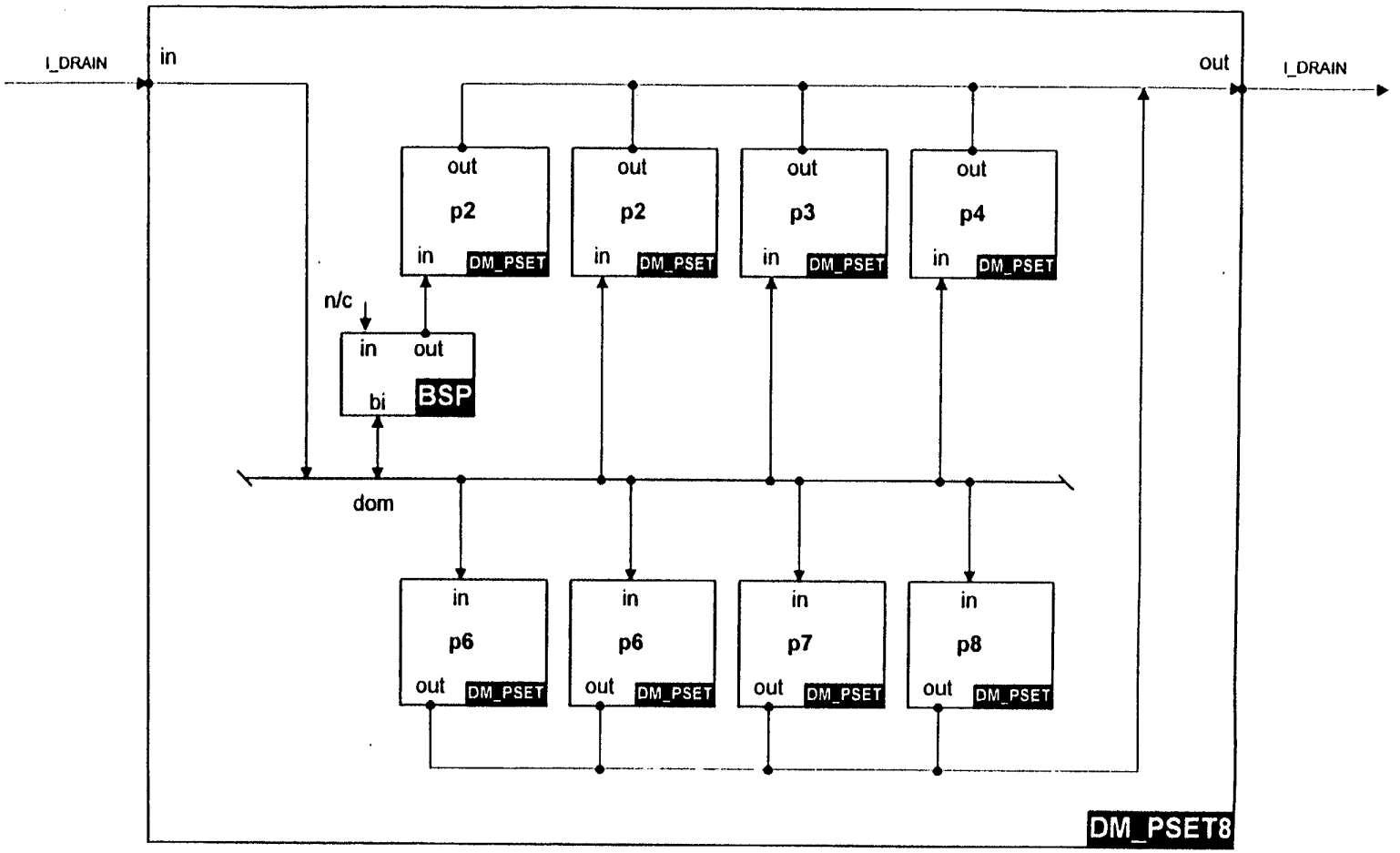

I_DRAIN
in
out
I_DRAIN
out
p2
in
DM_PSET
out
p2
in
DM_PSET
out
p3
in
DM_PSET
out
p4
in
DM_PSET
n/c
in
out
bi
BSP
dom
in
p6
out
DM_PSET
in
p6
out
DM_PSET
in
p7
out
DM_PSET
in
p8
out
DM_PSET
DM_PSET8

Fig. 135

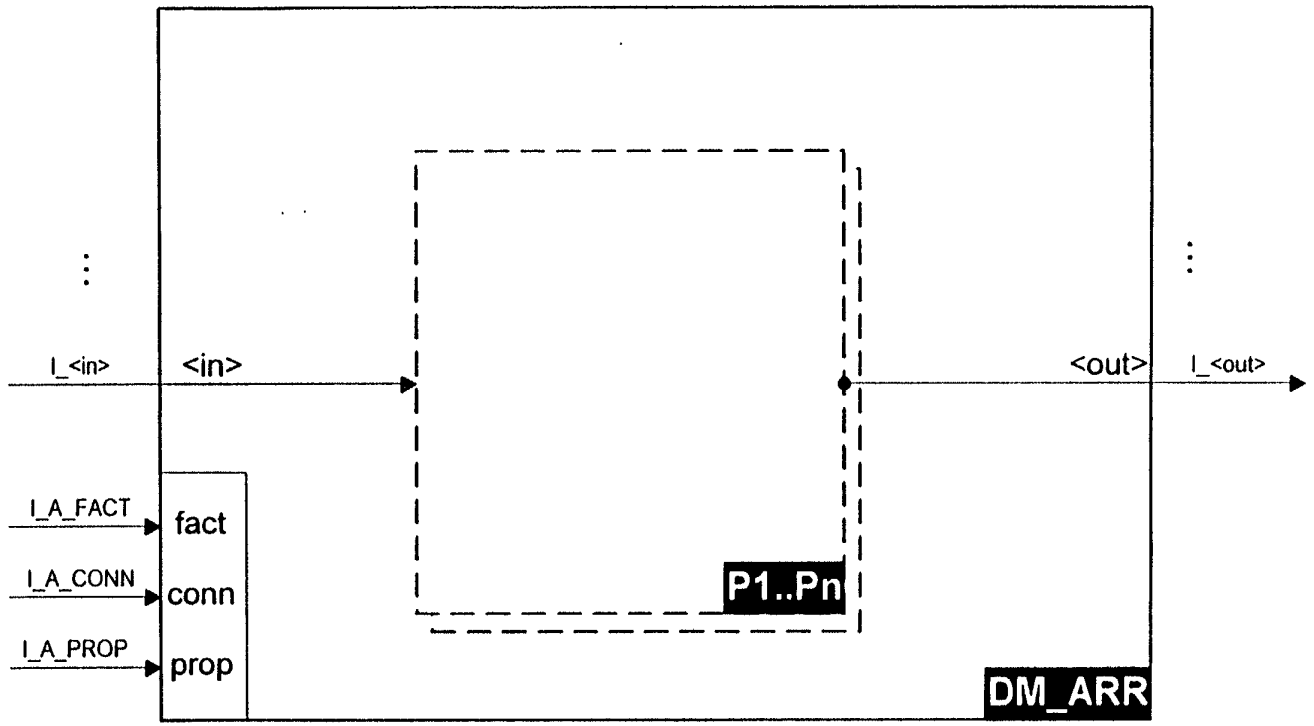

I_<in>
<in>
<out>
I_<out>
I_A_FACT
fact
I_A_CONN
conn
I_A_PROP
prop
P1..Pn
DM_ARR

Fig. 136

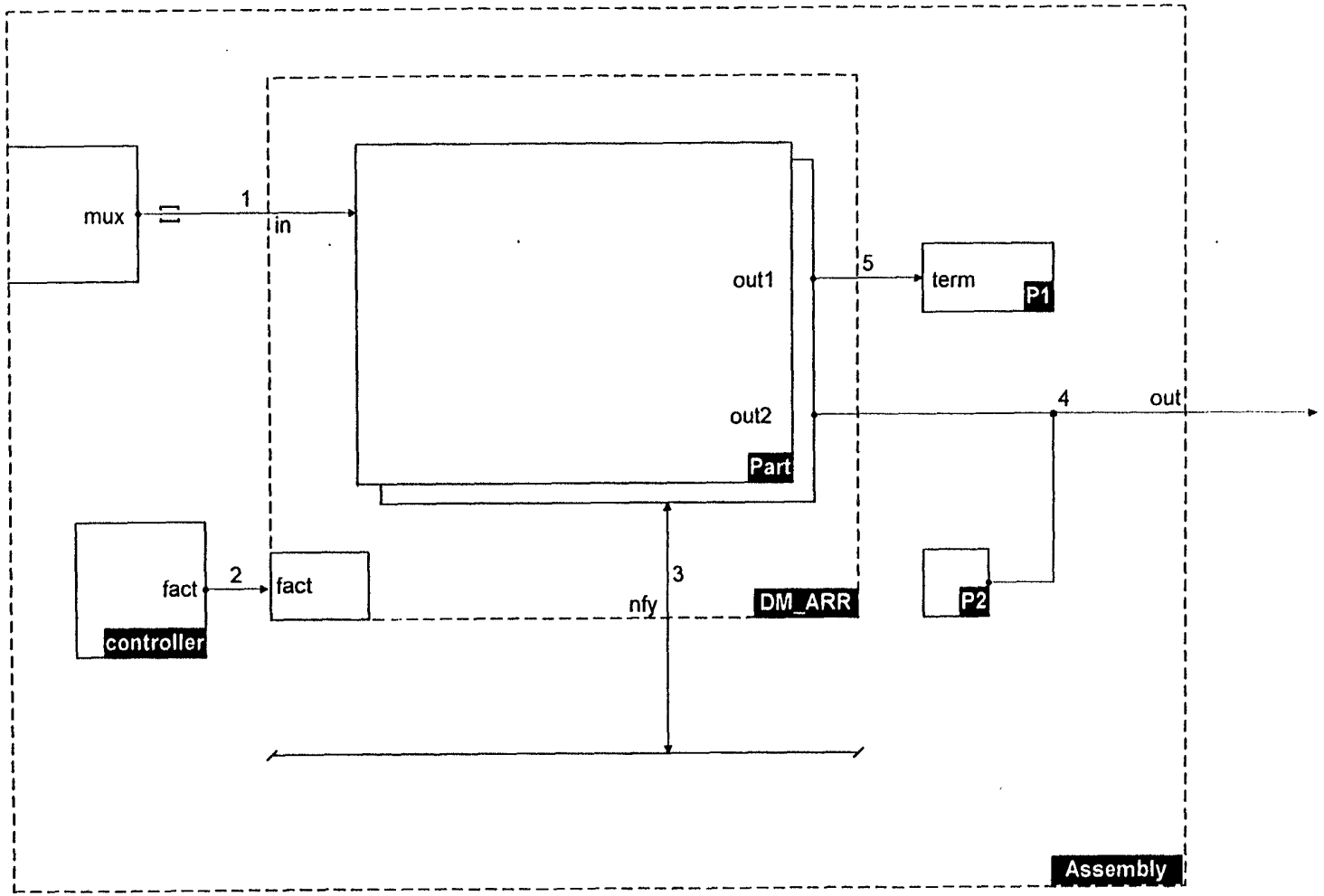

mux
1
in
out1
5
term
P1
out2
4
out
Part
fact
2
fact
3
nfy
DM_ARR
P2
controller
Assembly

Fig. 137

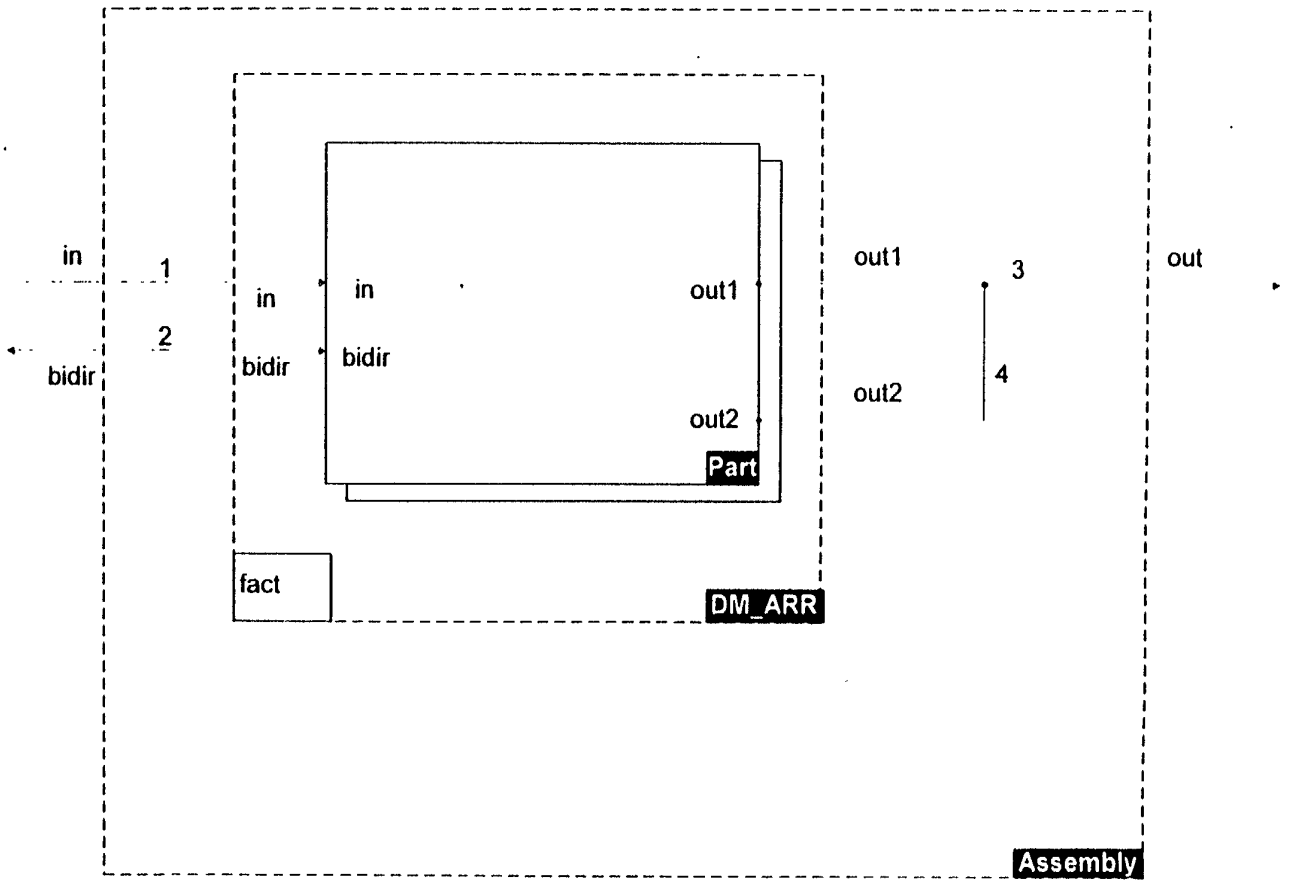

in
1
2
bidir
in
bidir
in
bidir
out1
out2
Part
fact
DM_ARR
out1
3
4
out2
out
Assembly

Fig. 138

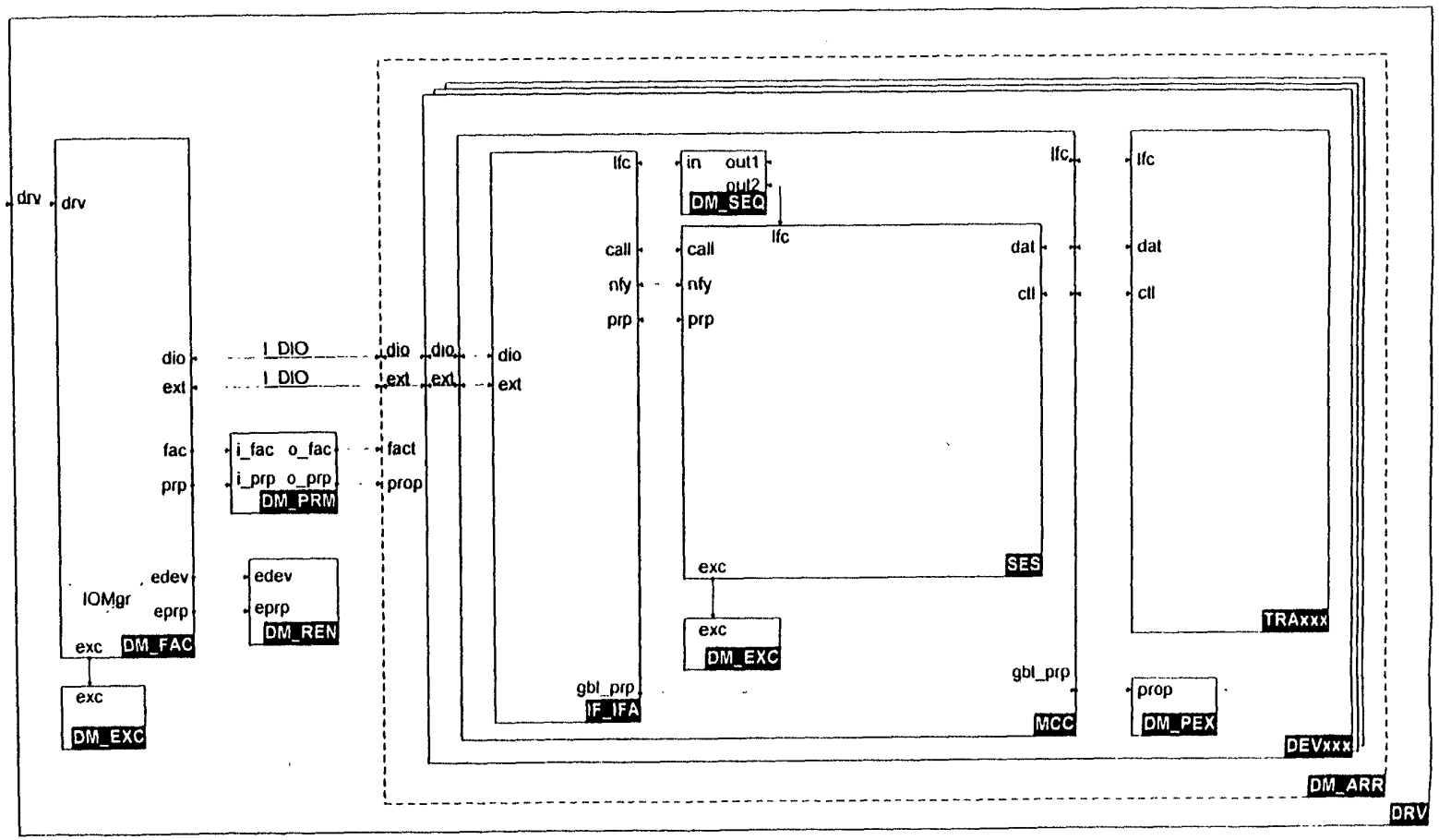

drv
drv
dio
ext
fac
prp
edev
eprp
IOMgr
exc
DM_FAC
exc
DM_EXC
I_DIO
I_DIO
i_fac o_fac
i_prp o_prp
DM_PRM
edev
eprp
DM_REN
dio
ext
fact
prop
dio
ext
dio
ext
lfc
call
nfy
prp
gbl_prp
IF_IFA
in out1
out2
DM_SEQ
lfc
call
nfy
prp
exc
SES
exc
DM_EXC
lfc
dat
ctl
gbl_prp
MCC
lfc
dat
ctl
TRAxxx
prop
DM_PEX
DEVxxx
DM_ARR
DRV

Fig. 139

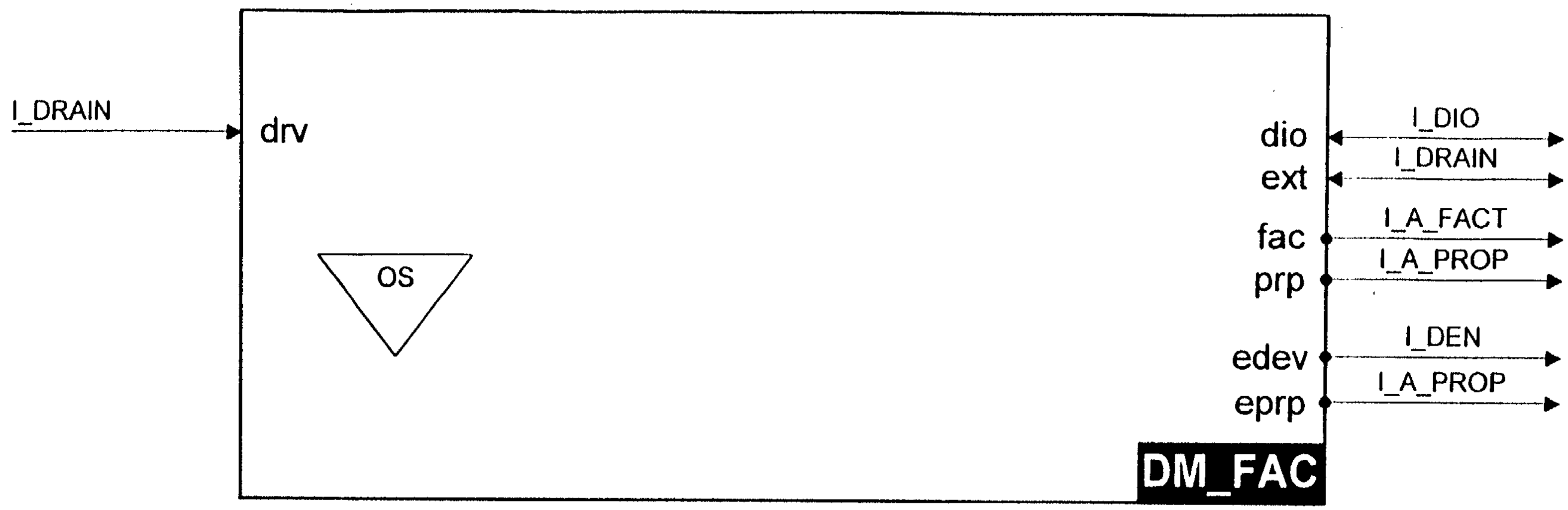

I_DRAIN
drv
OS
dio
ext
fac
prp
edev
eprp
I_DIO
I_DRAIN
I_A_FACT
I_A_PROP
I_DEN
I_A_PROP
DM_FAC

Fig. 140

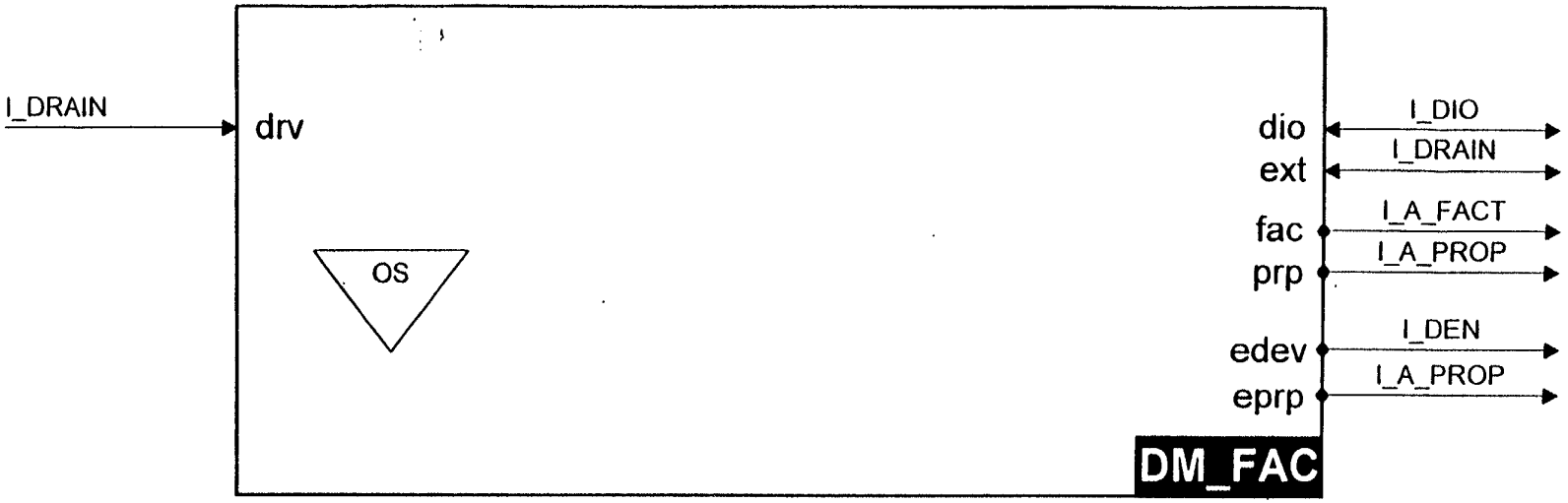


Fig. 141

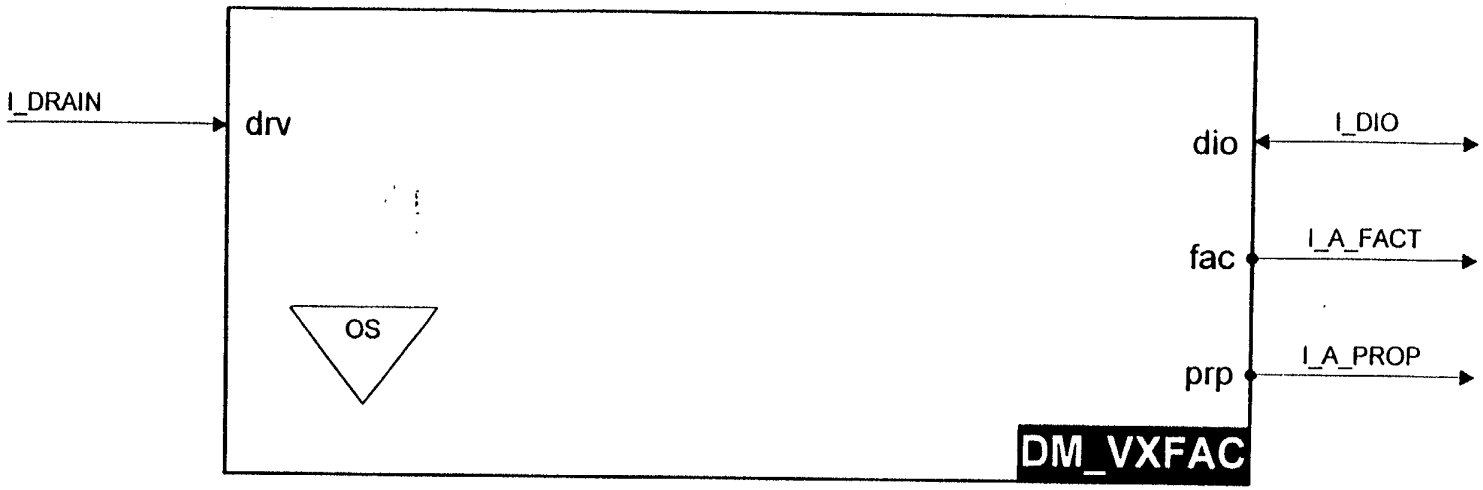


Fig. 142

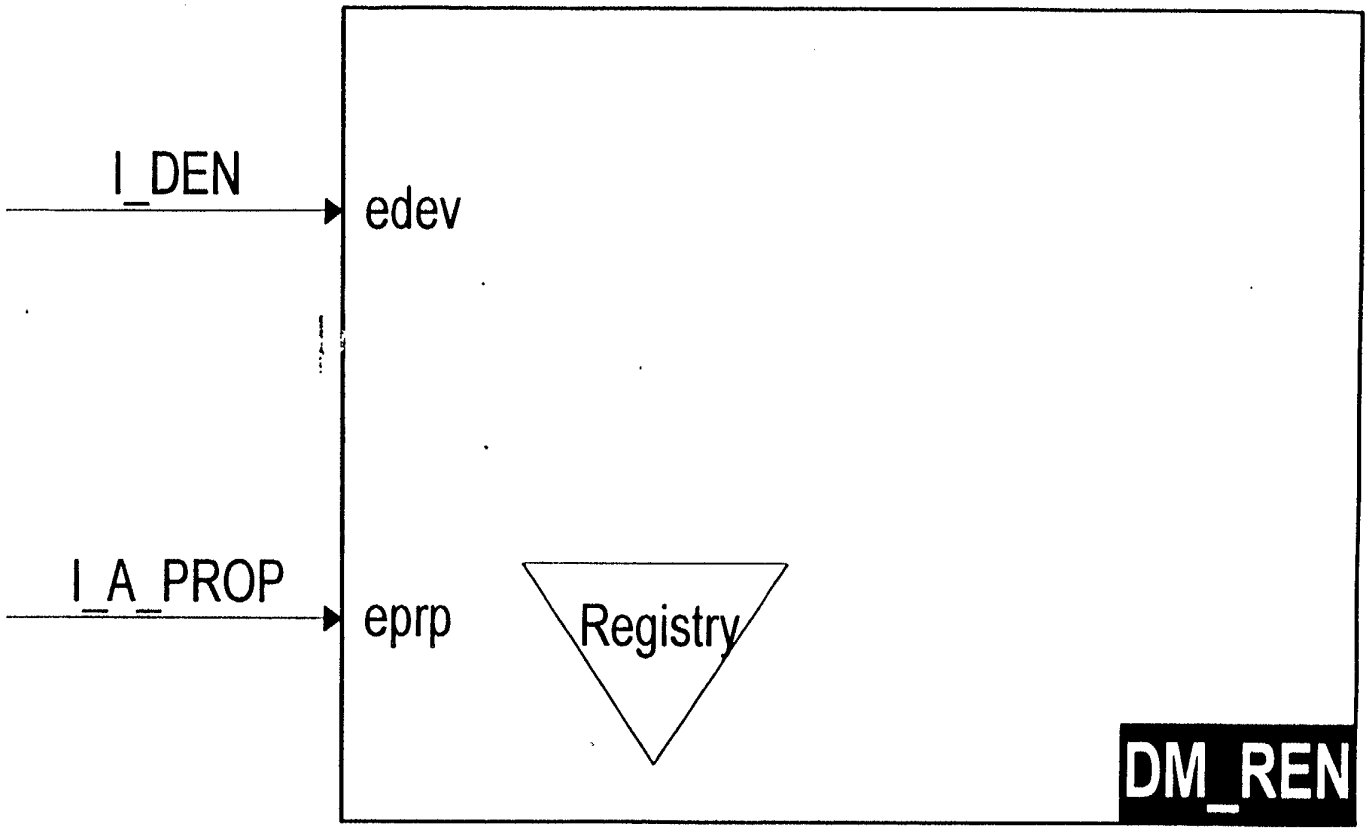


Fig. 143

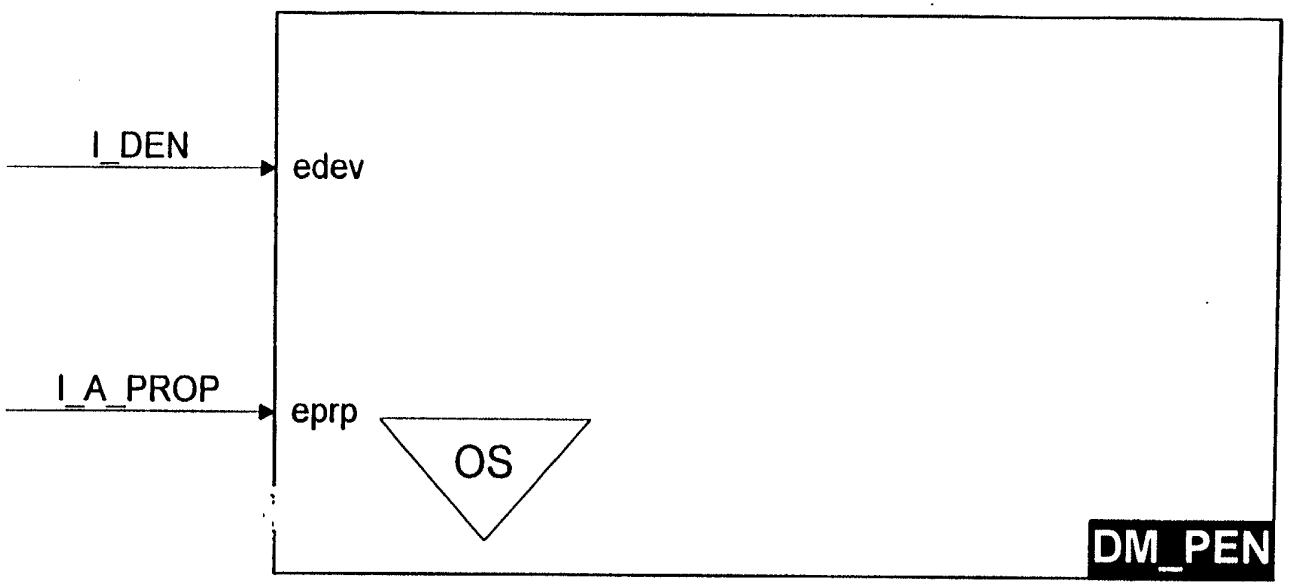


Fig. 144

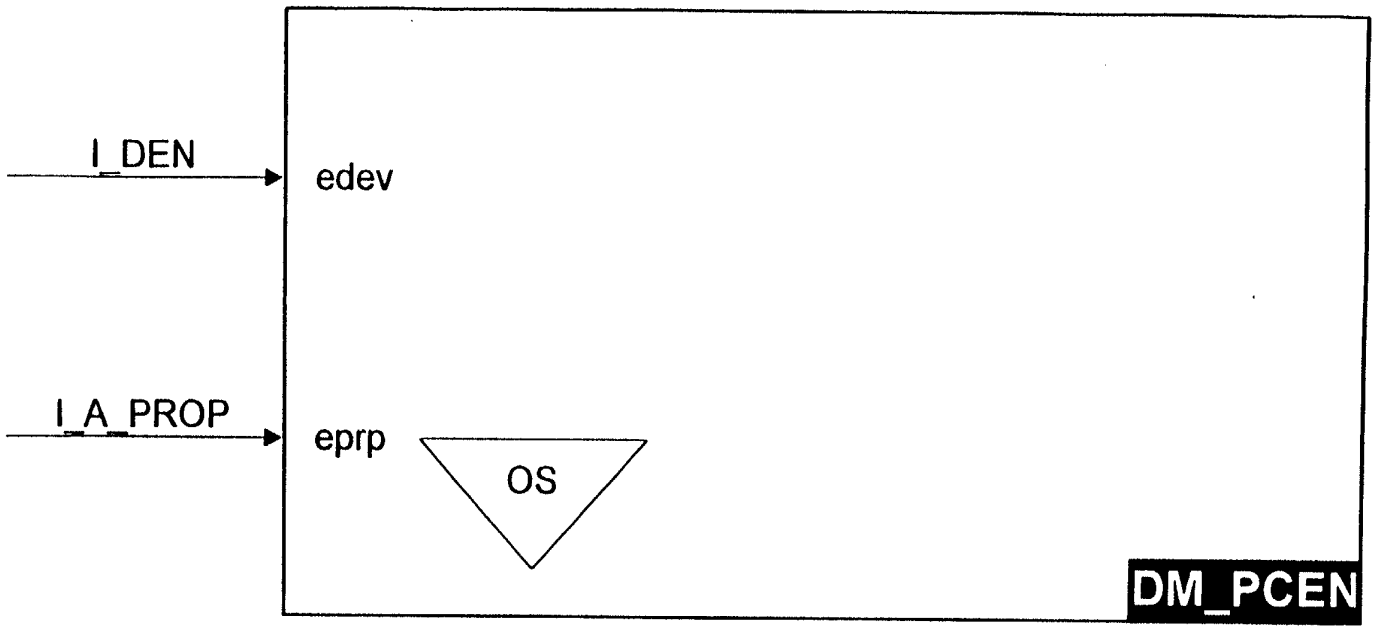


Fig. 145

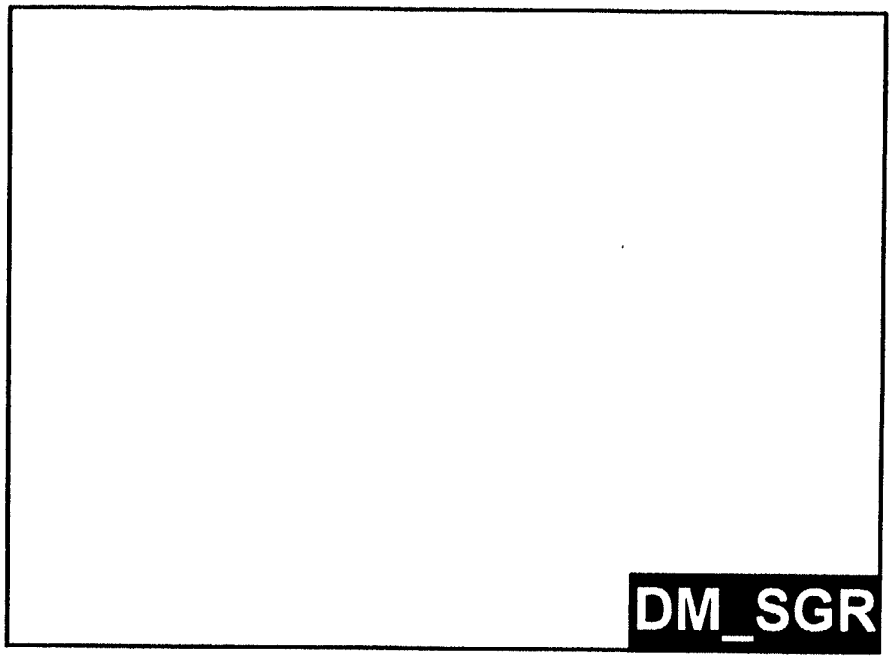


Fig. 146

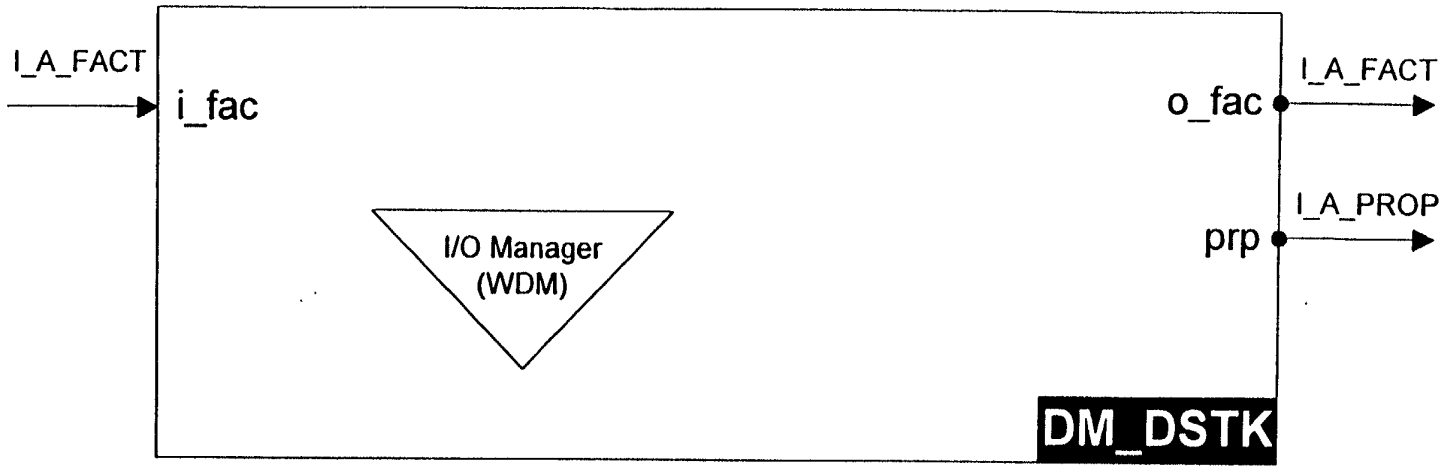


Fig. 147

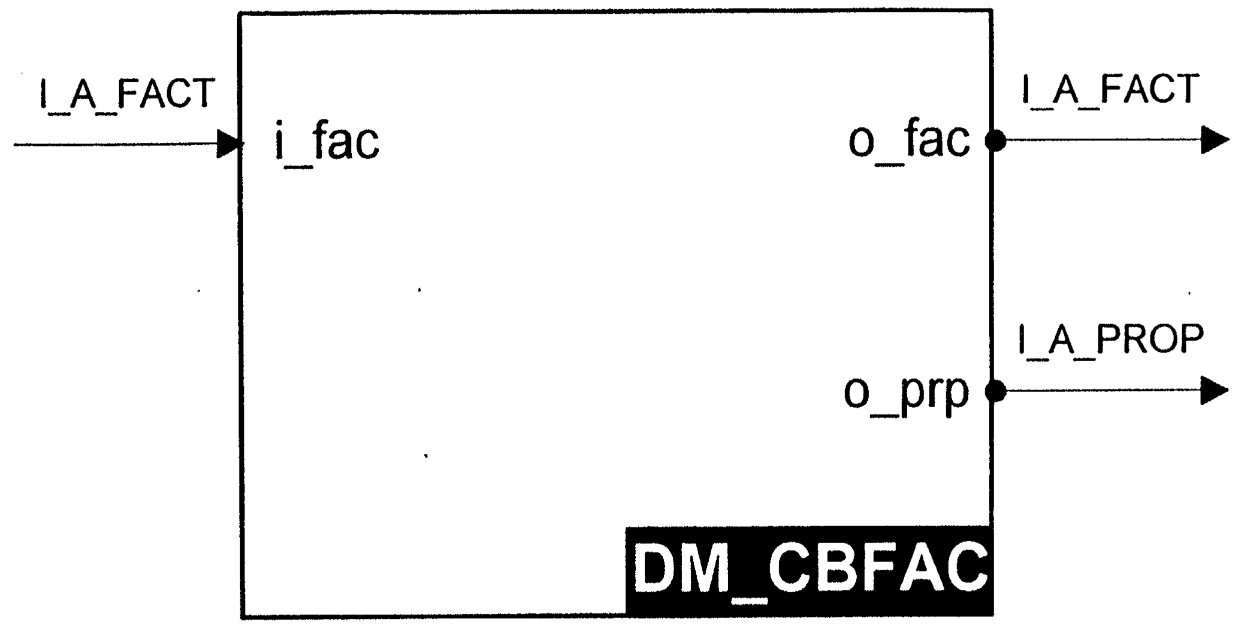


Fig. 148

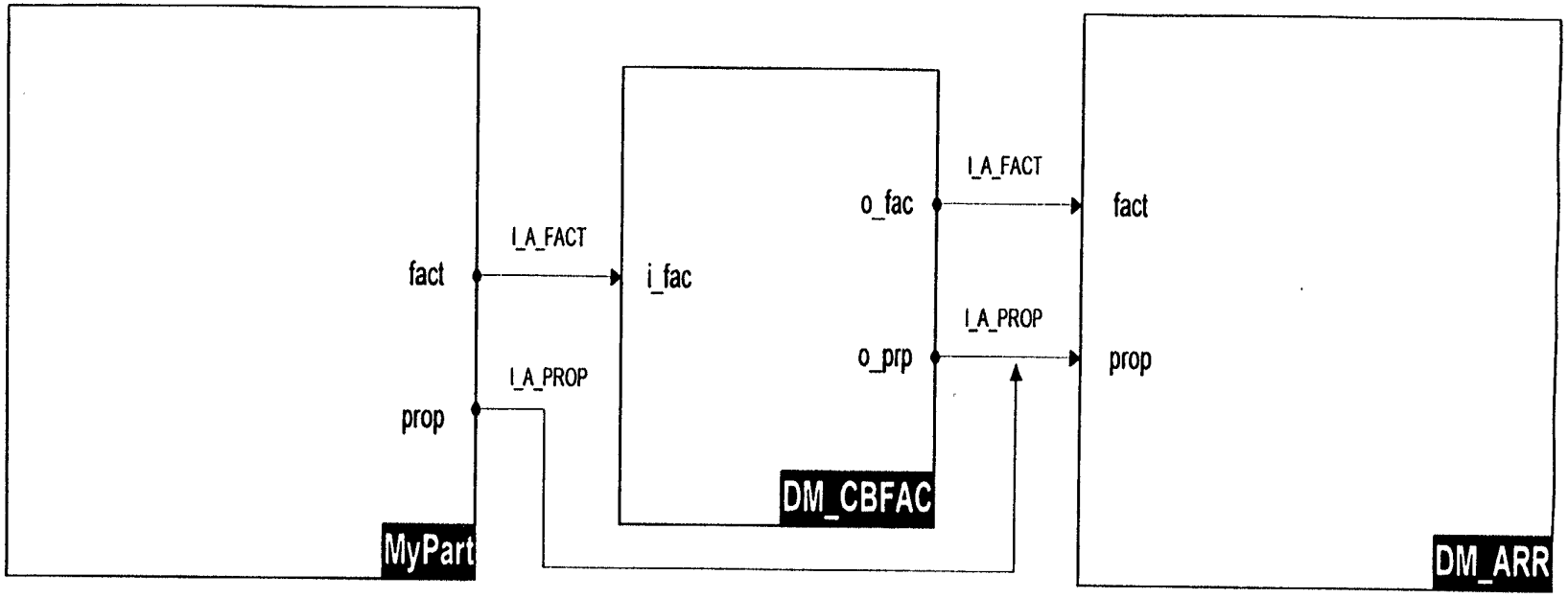

I_A_FACT
fact
I_A_FACT
i_fac
o_fac
I_A_FACT
fact
I_A_PROP
o_prp
I_A_PROP
prop
prop
DM_CBFAC
MyPart
DM_ARR

Fig. 149

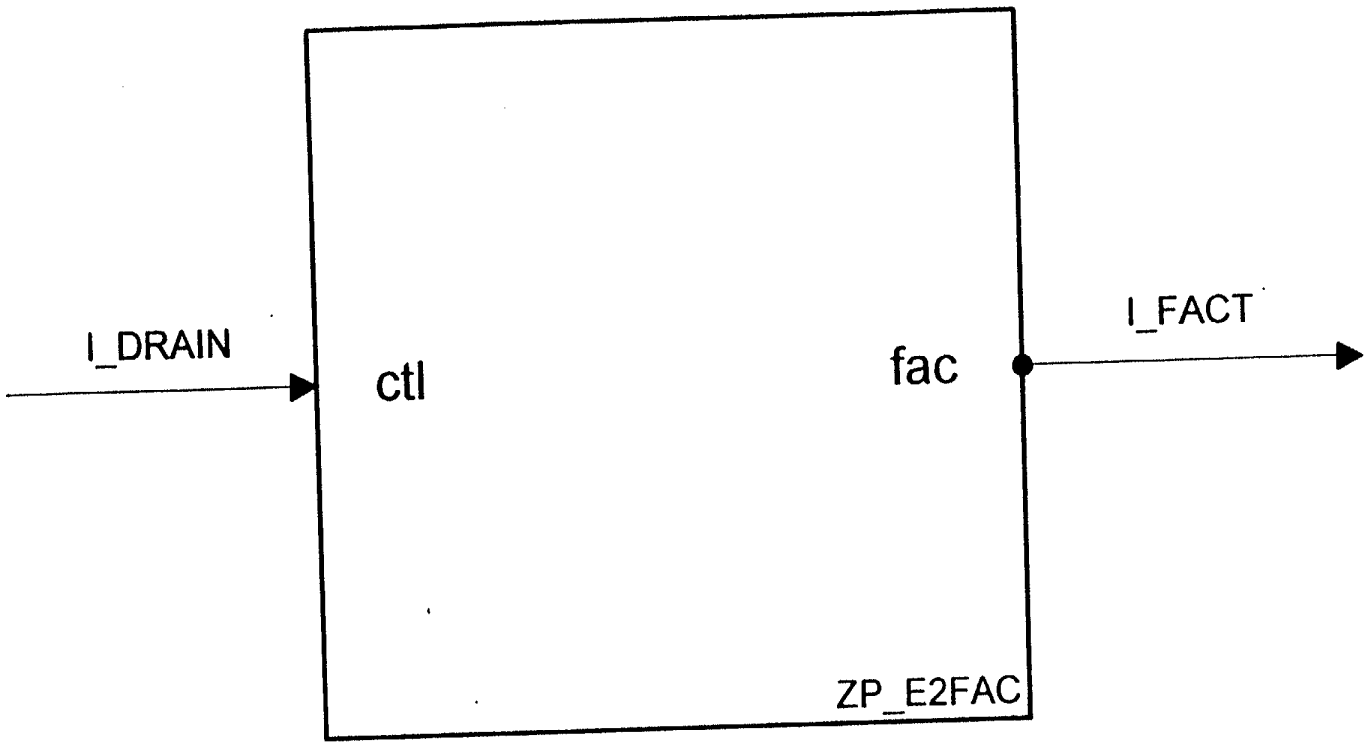


Fig. 150